Control Concepts for Hybrid Rectifiers Utilizing a Flying Converter Cell Active Current Injection Unit

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Abstract—A passive three-phase rectifier circuit equipped with a "Flying Converter Cell" (FCC) active current shaping network, based on the third harmonic injection concept, has been introduced recently. This additional/optimal circuit allows the upgrade of a standard B6 diode rectifier to a low harmonic input stage with unity power factor. In order to guarantee properly shaped sinusoidal mains input currents, dedicated current and voltage controllers of the active circuitry must be designed carefully. As the active current injection unit consists of an assembly of 3 individual converter stages, the design procedure of both current and superimposed voltage controllers results in fairly high complexity. It is therefore going to be discussed in detail in this work. Based on the analysis of the rectifier system an appropriate control concept is developed which is implemented using a digital signal processor. It is furthermore shown that the midpoint voltage of the FCC can advantageously be used for balancing of the DC capacitor stage of the cell without deteriorating THD of mains input currents. Measurement results taken from a 10 kW/10 kHz laboratory prototype finally confirm promising characteristics of the total hybrid system.

Index Terms—Three-Phase AC-DC Conversion, Third-Harmonic Injection, Current Control, Voltage Control, Voltage Balancing, Input Current Quality.

I. INTRODUCTION

In times of increasing power demand, active three-phase rectifier circuits are gaining more and more importance during the last decades. Especially applications as e.g. switch-mode power supplies and AC drives where increasingly (i) low harmonic input/line currents (THD < 5%), (ii) high power factor (PF > 0.99) and (iii) high efficiency (η > 95%) are mandatory ([1]), are of major concern. Numerous active rectifiers (as e.g. the Vienna Rectifier [2])) have been reported in literature which can achieve the mentioned requirements. Purely active rectifier systems, as e.g. the six-switch (active) rectifier, are state-of-the-art circuits for low voltage mains applications. Due to simplicity, robustness and low complexity the six-switch rectifier is widely used in industry and active components are available as combined power modules from numerous manufacturers. This topology however results in large volume of input inductors and shows limited maximum switching frequency (mentioned in [3]). The derived three-level topologies (i.e. NPC or T-Type) are characterised by reduced volume of passive components, lower switching losses and reduced voltage stress of switching devices. However, the mentioned topologies suffer from higher conduction losses and increased complexity compared to a two-level implementation. Active switching components of all these mentioned topologies, however, have to process the full active power. This issue can be reduced or overcome by some specific hybrid rectifiers which are only stressed by a small amount of active and reactive power.

Hybrid rectifiers e.g. employing third harmonic injection circuits (consisting of an active current shaping cell and an active current injection unit) can be separated into (i) active current injection/active current shaping (ii) passive current injection/active current shaping (iii) active current injection/passive current shaping (iv) passive current injection/passive current shaping. [4]–[18] mention different types of rectifier topologies applying the third harmonic injection principle whereas passive current injection/active current shaping is assumed. [4]–[8] and [10]–[13] discuss two different versions of the Minnesota rectifier. The first solution discloses DC-side located boost converter stages with additional passive third harmonic injection network. It can be implemented as series connected LC circuit, which is tuned close to the 3rd harmonic frequency. The second version considers a buck converter stage at the output of the rectifier, followed by a boost topology. The current injection network consists of a zig-zag transformer, which is connecting the injection path to each phase. These topologies, however, cannot serve as optional upgrade of passive three-phase rectifiers. Furthermore, both DC-DC converters have to process the main part of the active power. Hybrid rectifiers as discussed in [19]–[26] are classified by passive current injection/passive current shaping. In [22], the current injection network is implemented as simple and very well known star/delta transformer (whereas the secondary side of the transformer is short-circuited) and constitutes the interconnection between the AC- and the DC-side of the passive diode bridge rectifier topology. The third harmonic current is generated according to the instantaneous state of the passive rectifier and the design of the implemented passive components. A total harmonic input current distortion of < 5% is achievable if the ratio between third harmonic current i1 and output current Io is close or equal to 1 (i.e. io/Io). This can be accomplished e.g. by the use of a saturable reactor or a magnetic amplifier which however results in unfavorable complexity of the circuit.

A rectifier option considering active current injection/passive current shaping is explained in [25]. The proposed topology is an extension circuitry for three-phase diode bridge rectifiers consisting of an active current injection network (implemented as bidirectional switch arrangement) and a passive current shaping network (composed of 3 resistors and 2 capacitors).
tors). The system shows promising results for nominal load, however, appears to be inefficient for partial and light load operation.

On the contrary, hybrid rectifiers with active current injection/active current shaping (as proposed and/or discussed in [29]–[40]) serve as promising solutions to guarantee low harmonic input currents and a high power factor. All of these rectifiers are characterized by different attributes. Therefore, the proper selection of one specific rectifier highly depends on the given application, specifications and requirements (e.g. controllable output voltage buck - [32], controllable output voltage boost - [33], [34], upgradeable B6 rectifier - [35]–[38] (dependent on passive topology - e.g. AC-side, DC-side smoothing inductor) etc.). Another opportunity would be to apply flying capacitor converters on the AC-side of the system (as e.g. described in [41]). These rectifiers are able to provide bidirectional power flow. The FCC as described in this work is however only able to allow unidirectional power flow (predetermined due to the B6 rectifier topology). It has to be mentioned, that low harmonic input currents and unity power factor can also be achieved, if the active current shaping network is implemented as two flying capacitor converter branches in back-to-back connection. However, it must be considered, that each capacitor stage has to process 150 Hz and 300 Hz current components which leads to a relatively large capacitor volume (at least 4x600 V capacitor stages). Furthermore, additional capacitor balancing concepts are required.

This work is going to discuss a "Flying Converter Cell" (FCC - cf., Fig. 1) as proposed in [27] which can be used as additional/optional upgrade for a passive three-phase rectifier with LC output filter. The active optional upgrade only has to process some fractional amount of active and reactive power of the nominal transferred power. The main part of the transferred power is processed via the passive diode bridge rectifier (as already stated in [36] or [27]).

The active current injection topology consists of two half bridges (\(S_{cp}^{\pm}\) and \(S_{cn}^{\pm}\)) connected to the positive and negative busbar at the output of the passive diode bridge (\(D_1\)–\(D_h\)). The interconnection between B6 and FCC is formed via injection inductors (\(L_{cp}\), \(L_{cn}\) and \(L_{h3}\)) and a three-level bridge leg (\(S_{h3}\), \(D_{h3}^{\pm}\)). The three-level bridge is cyclically connected to one of the three mains phases (which shows 0 A gaps according to passive rectification) by three bidirectional switches (\(S_1\)–\(S_3\)). The third harmonic inductor \(L_{h3}\) forms the interconnection between AC-side connected bidirectional switches and DC-side located current injection cell. The FCC – which is able to achieve unity power factor and sinusoidal input currents – can furthermore be utilized as an extension/add-on-option for an already existing passive three-phase diode bridge rectifier (B6). A redesign of the passive topology is therefore not required. Only the enhanced circuit (FCC) has to be designed according to the input/output specifications of the passive system. Furthermore, no high-frequency common mode voltage (with switching frequency) appears at the DC-link output of the B6 (\(C_o\)) which can be noted as an additional advantage of a passive system equipped by an active FCC solution. Moreover, it has to be noted that the total system appears to be relatively robust, as in case of a malfunction of the active upgrade, the FCC can be turned off and the system is still further operable in B6 standalone mode.

However, as it is an upgrade for passive rectifiers, the output voltage of the system \(V_o\) cannot be controlled. \(V_o\) is still fixed according to the mains situation by \(V_o = 3\sqrt{3}V_{N} / \pi \approx 540 \text{ V} \) (for 400 VLL mains voltages). Additionally, 4-6 voltage and 3 current sensors are required. Compared to a typical AFE implementation, only one additional voltage sensor is necessary (3-level AFE: 5 voltage sensors – \(v_{Ni}\), \(v_{oP}\), \(v_{oN}\) and 3 current sensors – \(i_{pos}\), \(i_{neg}\), \(i_L\)).

In order to guarantee sinusoidal input currents the FCC has to compensate unfavorable 300 Hz current components of the output filter (\(L_{DC}\), \(C_o\)) of the passive system. Dedicated injection currents \(i_{cp}/i_{cn}\) are controlled such to achieve positive/negative 2\(\pi/3\)-sinusoidal wave shapes \(i_{pos}/i_{neg}\), respectively. The appropriate mains phase which instantaneously shows 0 A gaps is going to be fed by the generated third harmonic current \(i_{h3}\). Due to this required third harmonic injection additional shaping network the active cell unfortunately suffers from a very high number of active and passive switches. In order to be able to properly regulate the appropriate switching actions, the following sections are going to discuss dedicated current and voltage controllers, which are necessary for proper operation of the total system.

### II. Controller Design

Several controllers are required for proper operation of the proposed rectifier circuit. It is obvious that fast-acting current controllers are required to shape the mains currents. Next to the current controller also controllers for the FCC DC-link voltages are required. Besides mains voltages \(v_{Ni}\) also currents \(i_{pos}\), \(i_{neg}\) and \(i_L\) are measured as well as the rectifier output voltage \(v_{rec}\) and midpoint voltage \(v_{MN}\). As the output voltage \(V_o\) of the system is defined by the mains voltages \(v_{Ni}\) and is hence not controllable, sensing of \(V_o\) is not necessary.

Fig. 1: Active three-phase rectifier circuit utilizing a "Flying" converter cell as proposed in [27] and [28].
A. Current Control

In the following, the concept of average mode current control is used. The basic idea is to control the output currents $i_{pos}$ and $i_{neg}$ of the diode bridge (to the mentioned $2\pi/3$-periodically sinusoidal shape) by injecting adequate "compensational" currents $i_{cp}$ and $i_{cn}$ into the busbars as $i_{pos} = i_L - i_{cp}$ and $i_{neg} = i_{cn} - i_L$ applies. It is briefly shown, that sinusoidal input currents of all three mains currents can be achieved, if a proper current controller is going to be implemented. Therefore, one specific sector $\varphi_N \in \left[0 \ldots \frac{\pi}{3}\right]$ is chosen. In this sector, the positive and negative busbar currents yield

$$i_{pos}(\varphi_N) = i_{N1}(\varphi_N); \quad i_{neg}(\varphi_N) = i_{N3}(\varphi_N).$$

(1)

The injected currents $i_{cp}(\varphi_N)$ and $i_{cn}(\varphi_N)$ hence result in

$$i_{cp}(\varphi_N) = i_L(\varphi_N) - i_{pos}(\varphi_N) = i_L(\varphi_N) - i_{N1}(\varphi_N)$$

(2)

and

$$i_{cn}(\varphi_N) = i_L(\varphi_N) + i_{neg}(\varphi_N) = i_L(\varphi_N) + i_{N3}(\varphi_N).$$

(3)

According to Kirchhoff’s law the current $i_{h3}(\varphi_N)$ is defined by

$$i_{h3}(\varphi_N) = i_{cp}(\varphi_N) - i_{cn}(\varphi_N).$$

(4)

Considering all previously defined equations, injected current $i_{h3}(\varphi_N)$ for the specific sector results in

$$i_{h3}(\varphi_N) = i_{cp}(\varphi_N) - i_{cn}(\varphi_N)$$

$$= i_L(\varphi_N) - i_{N1}(\varphi_N) - i_L(\varphi_N) + i_{N3}(\varphi_N)$$

(5)

$$= i_{N2}(\varphi_N)$$

whereas the relation $i_{N1}(\varphi_N) + i_{N2}(\varphi_N) + i_{N3}(\varphi_N) = 0$ has been used. The current $i_{h3}(\varphi_N)$ is therefore equal to $i_{N2}(\varphi_N)$ in the respective sector. Detailed evaluations of all the other remaining sectors lead to similar results which proofs the operating principle of the proposed topology. The two half bridges are used for current control. The three-level bridge-leg is required for balancing of the FCC DC-link voltages and to control the average value of the midpoint voltage $V_{MN,avg}$ to zero. Two independent current controllers are used for $i_{pos}$ and $i_{neg}$. As already mentioned, the current $i_{h3}$ results due to subtraction of $i_{cp}$ and $i_{cn}$. For $\varphi_N \in \left[0 \ldots \frac{\pi}{3}\right]$ ($i_{N1}(\varphi_N) > 0; i_{N2}(\varphi_N), i_{N3}(\varphi_N) < 0$)

$$\delta_{cp}v_{cp} + v_{MN,avg} - v_{pos} = L_c \frac{di_{cp}}{dt}$$

$$\left(1 - \delta_{h3}\right)\left(-v_{cn}\right) + v_{MN,avg} - v_{mid} = -L_c \frac{di_{h3}}{dt}$$

(6)

$$\left(1 - \delta_{cn}\right)\left(-v_{cn}\right) + v_{MN,avg} - v_{neg} = -L_c \frac{di_{cn}}{dt}$$

can be calculated. Equal inductors ($L_c = L_{cp} = L_{cn} = L_{h3}$) are assumed for all three converter stages. In sector $\varphi_N \in \left[0 \ldots \frac{\pi}{3}\right]$, $v_{pos} = v_{N1}$, $v_{mid} = v_{N2}$ and $v_{neg} = v_{N3}$ applies. Furthermore, equal (constant) voltages $V_{cp} = V = V_c$ are assumed (which is valid due to DC voltage and voltage balancing controller) for the current controller design. Also the average value of the midpoint voltage $V_{MN,avg}$ can be treated as constant as it shows much smaller dynamic. Based on this simplification Laplace Transformation can be applied which finally results in e.g.

$$sL_c i_{pos} = sL_c i_L - \delta_{cp} V_c - V_{MN,avg} + v_{pos}$$

(7)

if $i_{cp}$ is going to be expressed by $i_{pos}$ and $i_L$. By inspecting Fig. 1 it is obvious that the upper half bridge of the FCC must generate an average voltage which equals the voltage difference $v_{pos} - V_{MN,avg}$ (where $v_{pos} = \max(v_{N1})$), which actually conforms in its waveform to the very well known three-phase passive rectifier positive output bus voltage with respect to mains neutral point). This voltage difference can easily be expressed if all input voltages are measured and hence be used as feed-forward signal. The current $i_L$ acts as a disturbance input of the current control loop and disturbance rejection can be applied if $i_L$ is measured. If the resulting feed-forward signal

$$\delta_{cp} = \delta_{cp} + \frac{v_{pos} - V_{MN,avg}}{V_c} + s \frac{L_c i_L}{V_c (sT_1 + 1)}$$

(8)

is used together with (7) the very simple current loop model

$$G_1(s) = \frac{v_{pos}(s)}{\delta_{cp}(s)} = -\frac{V_c}{sL_c}.$$  \hspace{1cm} (9)

can be obtained. The required differentiator block for $i_L$ has to be extended by a low-pass filter $T_1$ with higher cut-off frequency for noise suppression. In Fig. 2 the derived and advanced model in s- and z-domain (necessary due to signal sampling) is shown which is required for proper current controller design. The current controller $R_{P/P1}$ can be a P-type or a PI-type controller. A convenient PI-type controller design should also include occurring time delays (updated measured value to applied duty cycle, zero order hold ZOH, etc.). All quantities are therefore transferred into the continuous q-domain (also known as w-domain) using

$$G^\#(q) = G \left( \frac{1 + \frac{q}{T_2}}{1 - \frac{q}{T_2}} \right) \hspace{1cm} (10)$$

with $q = j\Omega$ and $\Omega = \frac{2}{T_s} \tan(\omega T_s/2)$. The applied bilinear Tustin transformation is the Padé approximation of the term $e^{j\Omega T_s}$. The double update PWM mode of the DSP can be advantageous be used in order to partially compensate the delay of the uniformly sampled PWM. The sample time $T_s$ is therefore defined by $1/(2f_s)$. The system should be designed such to achieve a rise time of $\approx 200 \mu s$ which results in an $\Omega_c$ of $6400 \text{rad/s}$ with $\Omega_{max} = 0.2 \cdot 2/T_s = 8000 \text{rad/s}$. Different controllers are designed for several maximum step response overshoot values of 10\%, 20\% and 40\% (as depicted in Fig. 2). The obtained quantities of $R_{P/P1}^\#(q)$ (current controller), and $T_{V1}^\#(q)$ (closed-loop transfer-function) have to be transformed back into the z-plane. It can be observed that, for a designed maximum overshoot of 40\% of the PI-type controller, actually a maximum overshoot of $\approx 50\%$ can be observed. This is mainly evoked due to the additional zero in the closed loop transfer function due to the $(qT_1 + 1)$-term of the PI-type controller and the purely integral behaviour of $G_1$. This effect can be compensated (or reduced) by using either pre-filtering technique, linear prediction $K_{LP}(z)$ or a Smith predictor. In order to verify proper controller design
The step response quality of the FCC is determined by the step response of the passive rectifier LC output filter. The dynamic of the developed (e.g. PT2) filter-type is hence be computed by using a digitally implemented low-pass filter. The dynamic of the developed (e.g. PT2) filter-type is going to define the step response quality of the FCC. The step response of the passive rectifier LC output filter is however affected according to the physical implementation of $L_{DC}$ and $C_o$. The stringently required digital low-pass filter therefore has to meet two different objectives. Firstly, the digital filter has to be able to compete with the dynamic behaviour of the passive LC filter. Secondly, it has to perfectly reject the passive power ripple. In case of insufficient damping, the generated nominal currents ($i_{2\text{mains}}$) and hence the mains input currents ($i_{N\text{mains}}$) will show increased $6^\text{th}$ harmonic spectral components and therefore an impaired THD$_{\text{i}}$. Fig. 3 depicts the voltage controller circuit with subsequent current controller. If an unduly lack of FCC system dynamic is considered, the FCC DC voltages $v_{cp}$ will show increased $6^\text{th}$ harmonic spectral components and therefore an impaired THD$_{\text{i}}$. In order to illustrate the discussed issue more accurate, a load step of the active system is briefly discussed. In case
of a load step of e.g. 10 kW to 3 kW the passive system immediately reacts with a response time of \(\approx 2\) ms (for e.g. \(L_{DC} = 2.25\ \text{mH},\ C_o = 1.1\ \text{mF},\ R_o,\ ESR = 0.23\ \Omega\) and \(R_{DC} = 0.3\ \Omega\)). If a first order 50 Hz digital low-pass filter structure is assumed for filtering of \(p(s)\) the proper output power is reached after \(\approx 100\) ms. Till then the difference of real \((p)\) and fictitious output power \((p + \Delta P)\) has to be processed by the FCC \((p_{FCC} = p + \Delta P - p)\). This additional power results in an increase of capacitor voltages \(v_{cp}\) and \(v_{cn}\) (if no appropriate voltage controller is applied) as FCC DC capacitors are going to be charged as long as \(p_{FCC} \neq 0\). The DC-link of the passive system remains almost constant (depending on the load characteristic) for such a load step. Similarly to previously made assumptions, discharging of the FCC DC-link capacitors applies for an increased load step of the system (e.g. 3 kW \(\rightarrow\) 10 kW). A load step can therefore be perceived by monitoring the FCC DC voltages \((v_{cp},\ v_{cn})\).

In order to guarantee not only a properly filtered output power but also a feasible system dynamic, the measurement circuit which evaluates the constant output power demand can be extended by a voltage control path. This voltage controller consists of a standard P-type regulator (to set the proper averaged DC voltage levels \(v_{cp} + v_{cn} = V_{\text{tot}}^*\) and \(\delta_{\text{cp}}\) and \(\delta_{\text{cn}}\) affects the quality of the mains input currents in the same manner as the previously discussed 300 Hz output power ripple. Considering all previously made assumptions and concerns, the voltage controller model can be derived and calculates to

\[
G_V(s) = \frac{V_{\text{tot}}^2}{\Delta P} = \frac{2}{sC_{cp}C_{cn}}.\tag{11}
\]

The P-type voltage controller gain can hence be easily computed according to the open-loop transfer function. According to Fig. 3, the closed-loop transfer-function of the slow responding path can be assessed by

\[
T_{y,v} = \frac{s + 1}{s^4\frac{\pi^2L_{DC}C_{\text{tot}}}{\text{180}v_T} + s^2\frac{\pi^2C_{\text{tot}}}{\text{180}v_T} + s + 1},\tag{12}
\]
with $V_1$ and $T_1$ as values of the designed PI-type current controller $V_1 (sT_1 + 1)/s$. Measurement results which compare calculated and measured step-response of the system will be finally illustrated in Fig. 10 in section III. Furthermore, only positive power flow is allowed due to passive diode bridge rectification. The total controller minimum output is hence limited to $P_{\text{min}} = P_o - \Delta P > 0$ W. The maximum limit of the voltage controller ($P_{\text{max}}$) mainly depends on physical constraints of the B6 bridge and the FCC active switches. The equivalent electric conductance $g_e^*$ can be determined by

$$g_e^* = \frac{P_o + \Delta P}{\sum_{i=1}^{3} i_{\text{eff}}^2 v^2_i}. \quad (13)$$

The reference currents of the FCC hence finally result in $i_{\text{pos}} = g_{v_{\text{pos}}} v_{\text{pos}}$, $i_{\text{h3}} = g_{v_{\text{h3}}} v_{\text{h3}}$ and $i_{\text{neg}} = g_{v_{\text{neg}}} v_{\text{neg}}$. The derived voltage control of the active system is however merely able to manipulate the total DC voltage level of the injection cell ($v_{\text{cp}} + v_{\text{cn}}$). In order to prevent imbalance of both voltages a DC voltage balancing concept has been derived in [42] which is briefly discussed in the following subsection.

### C. DC Voltage Balancing Concept

Imbalance of DC capacitor voltages typically results due to parasitic effects (e.g. capacitor leakage currents, interlock delay, unsymmetrical PWM signals, gate drives etc.). In order to evaluate the effect due to unsymmetrical parasitic components (e.g. capacitor ESR) considering unbalanced capacitor voltages, an extended model is required which includes inductor voltage drops ($v_{\text{Lcp}}, v_{\text{Lcn}}, v_{\text{Lh3}}$), DC ($R_{\text{DC,cp}}, R_{\text{DC,h3}}, R_{\text{DC,cn}}$) and equivalent series resistances ($R_{\text{ESR,cp}}, R_{\text{ESR,cn}}$) of coils and capacitors etc. Inductor voltage drops ($v_{\text{Lcp}}, v_{\text{Lcn}}, v_{\text{Lh3}}$) have to be considered due to the used rather low switching frequency (10 kHz). Consequently, significantly high inductance values ($L_{\text{cp}}, L_{\text{cn}}, L_{\text{h3}}$) are assumed. It has to be noted that design guidelines considering the active rectifier injection inductances are discussed in detail in [27]. A calculation of $I_{\text{cp}}$ or $I_{\text{cn}}$ is not possible in an analytical way, due to the definition of the currents $i_{\text{cp}}$ and $i_{\text{cn}}$ and has hence been determined numerically. The maximum current that needs to be regulated by an implemented active balancing concept can be assessed numerically to

$$I_{\text{cc,max}} = I_{\text{cp}} - I_{\text{cn}} \approx 1.5 \text{ mA} \left( P_o = 10 \text{ kW} \right) \quad (14)$$

for dedicated values $R_{\text{ESR,cp}} = 120 \text{ m}\Omega$, $R_{\text{ESR,cn}} = 180 \text{ m}\Omega$, $R_{\text{DC,cp}} = 152 \text{ m}\Omega$, $R_{\text{DC,cn}} = 163 \text{ m}\Omega$ and $R_{\text{DC,h3}} = 157 \text{ m}\Omega$. Remark that symmetrical DC and ESR values ($\Delta R_{\text{ESR,cp}} = R_{\text{ESR,cn}}$ and $\Delta R_{\text{DC,cp}} = R_{\text{DC,cn}} = R_{\text{DC,h3}}$) would lead to $I_{\text{cc,max}} = 0 \text{ A}$. Basically, detailed analyzes (of e.g. feasible switching states) revealed, that the midpoint voltage $v_{\text{MN}}$ can be utilized to achieve different currents in both DC-link capacitors $C_{\text{cp}}$ and $C_{\text{cn}}$.

A purely regulated offset can be employed to intensify or reduce hardly applied switching states of the FCC. However, adding a simple offset to all three duty cycles ($\delta_{\text{cp}}, \delta_{\text{cn}}, \delta_{\text{h3}}$) will permanently violate the upper boundary of $\delta_{\text{h3}}$ (’1’) and hence does not fit the requirements of an undisturbed current generation of $i_{\text{cp}}, i_{\text{cn}}$ and $i_{\text{h3}}$. This furthermore applies for all continuous functions as e.g. sinusoidal, triangular shaped waveforms etc. Therefore, a square wave signal due to its discontinuity (as shown in Fig. 4) is used to prevent $\delta_{\text{h3}}$ from exceeding its limit (’1’). An additional offset can now be added to the rectangular shaped modulation signal. The very simple midpoint voltage balancing algorithm ($v_{\text{MN}}^*$) can thus be written as $v_{\text{MN}}^* = v_{\text{amp}} \cdot \text{rect} (\phi_N) + v_{\text{off}}$ while $v_{\text{amp}}$ denotes the amplitude of the rectangular signal (rect ($\phi_N$)) and $v_{\text{off}}$ the adjacent offset. Fig. 4 illustrates most important voltage waveforms and currents $i_{\text{pos}}, i_1, i_{\text{cp}}$ and $i_{\text{h3}}$ of the system. The generation of the implemented nominal midpoint voltage is depicted in Fig. 5. The triangular shaped voltage $v_{\text{h3}}$ can be generated by measured mains voltages $v_{N1-3}$ and calculates to $v_{\text{h3}} = -\max (v_{\text{N1}}, v_{\text{N2}}, v_{\text{N3}}) - \min (v_{\text{N1}}, v_{\text{N2}}, v_{\text{N3}})$. The rectangular shaped signal (rect ($\phi_N$)) has to be formed such, that it has to reverse its sign each time $v_{\text{h3}}$ changes in sign ($\pm \pi/6$, $\pm \pi/3$, $\pm \pi/2$, $\pm \pi$). A detector in order to determine zero crossings of $v_{\text{h3}}$ is therefore necessary. An additional controller is necessary in order to compute the required voltage offset value ($v_{\text{off}}$).
Ideally, the calculated value has to equal the magnitude of the rectangular signal ($v_{\text{amp}} = v_{\text{off}}$) depending on the DC-link voltage situation ($\Delta V_c = v_{\text{cp}} - v_{\text{cn}}$). If e.g. $v_{\text{cp}}$ (instantaneous capacitor voltage of $C_{\text{cp}}$) shall be increased, a negative voltage offset is required. This negative DC offset will simultaneously lead to capacitor discharging of $C_{\text{cn}}$. In order to evaluate main characteristics of the proposed balancing algorithm a simplified model of the FCC was assumed (neglecting inductor voltage drops, parasitic components and resistances). Averaged currents for $C_{\text{cp}}$ and $C_{\text{cn}}$ can be found as

$$I_{\text{cp}} = \frac{1}{6} \cdot \frac{I_N \cdot v_{\text{off}} (18 + \pi^2 \sqrt{3})}{\pi V_c},$$

$$I_{\text{cn}} = -\frac{1}{6} \cdot \frac{I_N \cdot v_{\text{off}} (-18 + \pi^2 \sqrt{3})}{\pi V_c}. \quad (15)$$

Obviously, $I_{\text{cp}}$ and $I_{\text{cn}}$ conform to a linear dependency of $v_{\text{off}}$. The balancing algorithm is furthermore characterized by the rated output power which is indicated by $I_N$. The offset $v_{\text{off}}$ and the amplitude $v_{\text{amp}}$ of $v_{\text{MN,avg}}$ can hence not remain fixed for diverging loads. Assuming e.g. an offset ($v_{\text{off}}$) of 8 V (for 10 kW output power), $v_{\text{off}}$ has to be increased for partial and light loads to achieve similar induced capacitor currents due to decreased values of $I_N$.

In order to guarantee proper operation of the balancing concept the generated rectangular signal has to comply with a set of constraints which are going to be defined in the following. Considering $\delta_{h3}$ (cf. Fig. 6(a)), $v_{\text{amp}} > 0$ (1st constraint) and $v_{\text{amp}} \geq |v_{\text{off}}|$ (2nd constraint) has to be fulfilled. In order to use the maximum balancing capability, the offset $v_{\text{off}}$ should be chosen in the same size of the rectangular amplitude $v_{\text{amp}}$. $v_{\text{off}} = v_{\text{amp}}$ (3rd constraint). Considering $\delta_{\text{cp}}, \delta_{\text{cn}}$ positive and negative limits for the offset voltage $v_{\text{off}}$ can be determined to

$$v_{\text{off,lim}} = \pm \frac{V_c - \sqrt{3}V_N}{2} \left[ \frac{1}{2} \left( 1 + \frac{L_{\text{DC}}}{L} \right) \left( 1 \pm \frac{\pi}{2} \right) \right] - \frac{\omega L I_N}{2} \quad (16)$$

which eventually results in the 4th constraint. For $P_o = 10$ kW, $L_c$ of 2.6 mH, a DC-side smoothing inductance of 2.25 mH and FCC DC voltages ($V_c$) of 400 V, the maximum limit of the midpoint voltage offset $v_{\text{off,lim}}$ approximately results in 40 V. It has to be noted that equation (16) indicates, that even for no load mode of the active system, $v_{\text{off,lim}}$ is merely enlarging to 44 V. As previously mentioned, a rectangular shaped signal is required to prevent $\delta_{h3}$ from exceeding its upper limit (”1”). The occurring step characteristic (in all three duty cycles $\delta_{\text{cp}}, \delta_{\text{cn}}$ and $\delta_{h3}$) however causes small deviations in the modulation signals for $i_{\text{pos}}, i_{\text{neg}}$ and $i_3$ as the voltage controller of the three-level bridge leg can not ideally follow the implemented step. The unidirectional three-level bridge leg is therefore only able to increase or decrease the midpoint voltage of the FCC with a diminutive delay. It is therefore mandatory to keep $v_{\text{amp}}$ as small as possible to minimize current distortions, but high enough to guarantee minimum averaged currents for FCC capacitor voltage balancing. The adapted midpoint voltage has to be considered as feed forward signal for current controllers and midpoint voltage controller (cf., Fig. 2 and Fig. 5). The corresponding duty cycles ($\delta_{\text{cp}}, \delta_{\text{cn}}, \delta_{h3}$) for the dedicated current and voltage controllers, regarding deactivated voltage controller ($v_{\text{off}} = v_{\text{amp}} = 0$ V), generation of a positive voltage ($v_{\text{off}} = v_{\text{amp}} = 20$ V) averaged midpoint voltage $v_{\text{MN}}$ and causing a negative offset voltage ($v_{\text{off}} = -20$ V, $v_{\text{amp}} = 20$ V), are illustrated in Fig. 6(a). In contrast to [27] where inductance voltage drops are neglected, the duty cycles depicted in Fig. 6(a) are considering injection inductance voltage drops which obviously appear as mandatory side effects for low switching frequency (10 kHz) applications.

In Fig. 6(b) simulation results of the implemented balancing...
concept are shown. Both DC voltages $v_{cp}$ and $v_{cn}$, the averaged ($v_{MN,avg}$ - red), the nominal averaged ($v_{MN,avg}$ - blue) as well as the instantaneous ($v_{MN}$ - green) midpoint voltage are illustrated and depict charging and discharging cycles of the FCC capacitors $C_{cp}$ and $C_{cn}$. The spectrum of one mains phase input current ($i_{N1}$) regarding the implemented balancing concept compared to implemented ideal capacitors ($C_{cp} = \infty$) is finally visualized in Fig. 6(c). The THD$_i$ considering the ideal capacitor case was simulated to 1.85% and regarding voltage controller and balancing concept yields 1.86%. Hence, virtually no additional input current distortions for a range between 50 Hz and 2 kHz hence could be observed.

### III. EXPERIMENTAL RESULTS

Detailed specifications of the active system (shown in Fig. 7(a)), applied power semiconductor devices and passive components are given in TABLE I and TABLE II. The current injection laboratory prototype mainly consists of two different boards – controller and power board. The controller board contains measurement circuits, auxiliary power supply, DSP control unit (TI 320F2808) and additional hardware as e.g. zero crossing detection of mains line-to-line voltages and bidirectional switch controller (Lattice CPLD – MachXO 2280).

The power board, includes main power components as heatsink, IGBTs, gate drives, input filter, current sensors, electrolytic capacitors and further electric circuits which are required for e.g. proper start-up operation of the system. The system has been designed for 400 V$_{LL}$/50 Hz mains

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**TABLE I: Design Specifications of the Built Three-Phase Rectifier using a FCC.**

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mains voltage:</td>
<td>$V_{LL} = 400\text{ V}_{\text{rms}}$</td>
</tr>
<tr>
<td>Mains frequency:</td>
<td>$f_N = 50\text{ Hz}$</td>
</tr>
<tr>
<td>Switching frequency:</td>
<td>$f_s = 10\text{ kHz}$</td>
</tr>
<tr>
<td>FCC DC-link voltage:</td>
<td>$V_{cp} = V_{cn} = 400\text{ V}$</td>
</tr>
<tr>
<td>Output power:</td>
<td>$P_o = 10\text{ kW}$</td>
</tr>
</tbody>
</table>

**TABLE II: Power Devices Selected for Implementation of the FCC Prototype.**

<table>
<thead>
<tr>
<th>Device</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_{ia,b}$</td>
<td>1200 V/40 A IGBT, IKW40T120, Infineon</td>
</tr>
<tr>
<td>$S_{cp}$</td>
<td>600 V/20 A IGBT, IKW20N60H3, Infineon</td>
</tr>
<tr>
<td>$D_{h3}\pm$</td>
<td>1200 V/15 A, STTH1512W, ST-Microelectronics</td>
</tr>
<tr>
<td>$C_{cp}$</td>
<td>470 $\mu$F/400 V, EPCOS B43501-type</td>
</tr>
<tr>
<td>$L_{cp}=L_{cn}=L_{h3}$</td>
<td>3.2 mH, Iron core 3U60a, N = 123 turns</td>
</tr>
<tr>
<td>$C_F$, $C_S$</td>
<td>6.8 $\mu$F/275 V AC, MKP X2, Arcorotronics</td>
</tr>
<tr>
<td>$C_D$</td>
<td>2.2 mF/400 V, Felsic CO 39 A728848</td>
</tr>
<tr>
<td>$L_{DC}$</td>
<td>2.25 mH, Iron core 2 x U60a</td>
</tr>
<tr>
<td>$D_1 - D_6$</td>
<td>35 A/1600 V, 36MT160, Vishay</td>
</tr>
</tbody>
</table>

---

**Fig. 7:** (a) Constructed 10 kW laboratory prototype of the FCC and used three-phase choke. Dimensions FCC: 300 mm x 200 mm x 97 mm and three-phase choke 120 mm x 50 mm x 100 mm. (b) Simplified schematic of implemented hardware prototypical concept of the FCC rectifier.

**Fig. 8:** (a) Measured power factor $\lambda$ and input current quality (THD$_i$) as a function of output power. (b) Measured efficiency $\eta_{\text{meas}}$ of the laboratory prototype for a mains voltage of $V_{LL} = 400\text{ V}$. 

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Fig. 9: (a) Mains currents $i_{N1}, i_{N2}, i_{N3}$ and mains voltage $v_{N1}$ during 10 kW steady state operation ($\text{THD}_i = 2.3\%$, $\lambda = 0.998$). (b) Positive busbar current $i_{\text{pos}}$, injection current $i_{cp}$, DC-side smoothing inductor current $i_L$ and output voltage $v_o$ for 2.6 kW partial load operation. (c) Positive and negative busbar current $i_{\text{pos}}$ and $i_{\text{neg}}$, injection current $i_{h3}$ and mains voltage $v_{N1}$ for 1.7 kW partial load operation.

Fig. 10: Measurement results taken from the laboratory prototype for nominal output power (10 kW). (a) Input current waveforms for transition from passive diode mode operation (B6 standalone mode) to active current shaping (FCC activated). (b) Transition from passive diode mode operation to active current shaping using the proposed voltage control and balancing concept ($v_{\text{off}} = \pm 10\text{ V}, v_{MN} = \pm 10\text{ V}$). (c) Steady state operation while deactivating the voltage balancing controller and reactivating it after 1 s.

Fig. 11: Load step characteristics of the implemented rectifier system. (a) Input current characteristics for a 10 kW to no load operation (0 W) step. (b) Current and voltage characteristics for a 10 kW to 5 kW and a (c) 5 kW to 10 kW load step.

voltages, which results in 400 V DC voltage levels for the injection cell capacitors $C_{cp}$ and $C_{cn}$ (if a modulation index $M = 0.8125 = V_N/V_{cp}$ is assumed). The relatively low DC voltage of the switching cell furthermore allows the implementation GaN or SiC-MOSFETs which are recently available for blocking voltages $>400$ V (e.g. ROHM’s SCT2120AF, or GaN Systems’ GS66508T). This offers an operation with increased switching frequency with lower switching losses compared to a conventional IGBT. The SiC-MOSFET, furthermore, shows ohmic characteristics which will result in improved conduction losses (compared to an Si-IGBT). The implementation of a SiCMOSFET can hence lead to a smaller and less expensive cooling system/volume (if SiC conduction and switching losses are smaller than that of
an IGBT). The bidirectional switches can also advantageously be implemented by e.g. 900 V or 1200 V SiC-MOSFETs in order to reduce losses of the current injection stage (higher expense has to be taken into account). For proper operation, 6 voltage (line-to-line voltages or $v_{N1}$, $v_{cp}$, $v_{cn}$ and $v_{MN}$) and 3 current sensors ($i_{pos}$, $i_{neg}$ and $i_L$) are required. Also a 5 voltage sensor solution would be possible if the third mains phase is calculated by the already measured two remaining ones. A simplified schematic of the implemented concept of the FCC rectifier is depicted in Fig. 7(b). It is shown that software algorithms as current/voltage controllers, start-up sequence (SU), and state machine (SM) are implemented in the digital signal processing unit. The dsp is generating the duty cycles with switching frequency for both half bridges and the three-level bridge leg. A CPLD is furthermore required, as the bidirectional switches have to initiate their commutation at the same time instant when the B6 diodes are commutating. A delay which is as small as possible is a stringent requirement in order to prevent input current distortions of the total system. The very fast updating CPLD is hence necessary which has to evaluate the proper (100 Hz) switching sequence dependent on the mains voltage situation. Moreover, the CPLD can be used to realize the required dead time of generated PWM gate signals $g_{cp+}$ and $g_{cn+}$ (of appropriate switches $S_{cp+}$ and $S_{cn+}$, respectively).

Basic measured characteristics (efficiency $\eta_{\text{meas}}$, total harmonic distortion of input currents THD$_i$ and power factor $\lambda$) of the rectifier system dependent on the provided output power are illustrated in Fig. 8(a) and Fig. 8(b). Regarding efficiency rates, a maximum rectifier efficiency of 97.8% can be read at the nominal output power of 10 kW. It has to be noted, that the efficiency of the passive diode rectifier for the same load in B6 standalone operation has been obtained with 98.7%. The assembled rectifier system furthermore achieves a THD$_i$ below 5% down to a output power of $\approx$ 3 kW. Also a power factor above 0.95 is measured for an output power above 2.2 kW. The constructed FCC shows a good performance even for partial load condition ($P_o = 5$ kW) where a THD$_i$ of 2.7% and a power factor of $\lambda = 0.992$ can be measured at a good efficiency of $\eta_{\text{meas}} = 97.5\%$. As can be observed, the efficiency is decreasing for light load operation (e.g. 95% for an output power of 1.7 kW). This effect is mainly evoked due to the DC-side smoothing inductance current $i_L$. This current can be of negative value if the FCC is operating, as the FCC is able to process both, positive and negative current values. For light- and no-load condition, fractions of $i_L$ hence occur as circulating current which has to be processed by the FCC, the DC-side smoothing inductor ($L_{DC}$) and the DC-link voltage capacitor ($C_v$). This circular current causes additional losses compared to a passive standalone system during no-load operation (inductor losses $L_{DC}$ and $L_c$, switching and conduction losses etc.).

The three mains currents $i_{NI}$ and phase voltage $v_{N1}$ are shown in Fig. 9(a) for the nominal output power $P_o = 10$ kW of the constructed laboratory prototype. The implemented PI coefficients for a switching frequency of 10 kHz, double updated PWM mode and a maximum overshoot of 25% resulted in $R(z) = (0.145 - 0.1373z^{-1})/(1 - z^{-1})$. The currents show (as already discussed) a THD$_i$ of 2.3% and a power factor of $\lambda = 0.998$ can be read. Please note that mains voltages already show a THD$_i$ of 1.7%.

Fig. 9(b) and Fig. 9(c) illustrate measurement results of most important injection an regulated currents for 2.6 kW and 1.7 kW, respectively. Furthermore, also the output voltage $v_o$ of the system is depicted. It is only characterized by the typical 100 Hz (according to unbalanced input voltages) and 300 Hz spectral components (very well known from the passive three-phase rectifier topology). The output voltage (which cannot be controlled and is defined according to the mains voltage situation) for $400\, V_{LL}$ input voltages has been obtained with 529 V. As already discussed, Fig. 9(b) depicts the mentioned negative values of $i_{Lcp}$ and $i_{Lcn}$. The appearing circulating current then results in a reduced system efficiency at light-load and/or no-load condition.

Measurement results of the FCC voltages and input currents during the transition from B6 standalone mode to active regulated FCC operation are depicted in Fig. 10(a) and Fig. 10(b). The transition from passive to active diode bridge mode and the appropriate charging of the FCC DC voltage from 280 V (pre-charged) to 400 V required for proper generation of injection currents for each half bridge switching leg, are therefore illustrated. The used voltage controller gain is defined by $k_{cp,v}=0.025$ (crossover frequency 17 Hz). After the DC voltages are set to the dedicated 400 V limit they are perfectly balanced ($v_{cp} = 399.8$ V, $v_{cn} = 400.1$ V). Fig. 10(b) furthermore illustrates a smooth transition of both FCC DC voltages $v_{cp}$ and $v_{cn}$ without any perceivable overshoot, while active voltage balancing is operating. The DC voltage balancing concept is verified in Fig. 10(c). For the proposed balancing concept both DC voltages of the FCC are perfectly aligned. After deactivating (white area in Fig. 10(c)) the balancing algorithm ($v_{\text{amp}} = v_{\text{eff}} = 0$ V) $v_{cp}$ and $v_{cn}$ are starting to drift off the required voltage level of 400 V ($V_{cp} = 435$ V, $V_{cn} = 365$ V). Reactivating the balancing concept finally regulate the FCC DC voltages to the expected 400 V voltage level.

Fig. 11(a-c) illustrate different load steps for of the rectifier system. Fig. 11(a) depicts a full load step from nominal power (10 kW) to no-load operation of the system. As can be seen, during no-load operation there are still input currents drawn by the system which mainly appear due to input filter capacitors (6.8 $\mu$F), dedicated filter RC damping network (3 $\Omega$, 6.8 $\mu$F) and to cover system losses according to circulating currents, balancing output resistors, etc. Furthermore, the total FCC DC-link voltage $v_{\text{tot}}$ is illustrated in Fig. 11(b) and Fig. 11(c) for decreasing (10 kW to 5 kW) and increasing (5 kW to 10 kW) load steps, respectively, while taking advantage of the previously discussed implemented voltage controller structure. It can be observed that the voltage deviation of the total FCC DC voltage link is defined by approximately 40 V which is about 5% of the defined rated voltage level $V_{\text{tot}}^* = V_{cp}^* + V_{cn}^* = 2 \cdot 400$ V $= 800$ V. 
IV. CONCLUSION

In this work dedicated control concepts for hybrid rectifiers employing a FCC (which basically acts as optional current injection unit) is discussed. The total control structure including current controller (inner loop) and voltage controller (outer loop) is presented. The proposed concept is theoretically and mathematically analyzed. Current controllers can be easily realized by a simple P/PI-type controller if \( v_{\text{pos}} \), \( v_{\text{MN,avg}} \) and \( i_L \) serve as feedforward signals.

FCC DC voltage control, which can be separated into total FCC voltage control (\( v_{\text{CP}} + v_{\text{CN}} = 2V_c \)) and FCC balancing controller (\( v_{\text{CP}} - v_{\text{CN}} = 0 \)) is furthermore discussed. Emerging issues (low-frequency distortions regarding THD, and lack of dynamic compared to a conventional passive rectification system with LC output filter) due to inappropriate digital filter concepts are addressed, which obviously require non-linear control concepts for compensation. The voltage balancing concept advantageously uses the midpoint voltage \( v_{\text{MN}} \) of the FCC to charge or discharge the DC voltage capacitors. Both, current and voltage controller concepts have been implemented in a digital signal processor of a 10 kW/10 kHz laboratory prototype. Measurement results revealed that derived concepts are well suited for the proposed converter topology.

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REFERENCES


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