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Impact of Defect-Induced Strain on Device Properties

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A significant increase of the drain current appears if defined arrangements of dislocations are present in the channel of MOSFETs. Furthermore, analyses of the electronic properties of individual defects refer to a supermetallic behavior of dislocations. The reason is the extremely high strain in the dislocation core exceeding values of $\varepsilon \cong 0.1$. Such high strain causes substantial changes of the band structure and means that dislocations represent quantum wires. Quantum mechanical device simulations based on this conclusion demonstrated the transport of carriers on dislocations. The effect of gate voltage and strain in the dislocation core was analyzed in detail.

Crystal defects might have detrimental impacts on electrical parameters of semiconductor devices. Therefore, numerous comprehensive strategies were developed to avoid growth- and process-induced defects such as point defects, dislocations, grain boundaries, and precipitates.[1,2] Further, scaling combined with novel processing techniques, however, introduce new crystal defect phenomena[3,4] An individual defect, for instance, may already cause device failures by decreasing feature size below 20 nm. Furthermore, the integration of dissimilar materials into specific device regions is a main reason for defect generation. For instance, high mobility channel materials, as Ge, SiGe, or III–V compounds, are of growing interest[5,6] having different lattice constants to the substrate resulting in high local strains and may induce the generation of dislocations. Therefore, the knowledge about the electronic structure of individual defects is an important issue for next generation nanodevices.

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The present paper deals with investigations of the electronic structure of dislocations in silicon. Dislocations represent one-dimensional crystal defects. It is demonstrated that defined arrangements of dislocations exhibit numerous exceptional electronic properties characterizing these defects as nanowires embedded in a perfect crystalline matrix. The modified electronic properties are due to the very high strain inside the defect core resulting locally in strong modifications of the band structure.

The technique to realize defined two-dimensional arrays of dislocations in thin layers (semiconductor wafer direct bonding) was described elsewhere.[7,8] Silicon-on-insulator (SOI) wafers (diameter 150 mm, buried oxide (BOX) thickness 60 nm, device layer thickness 30 nm) were used for the wafer bonding process under hydrophobic conditions. One of the handle wafers was removed after bonding resulting in a new SOI wafer having a device layer thickness of 60 nm and a two-dimensional dislocation network in the middle. SOI MOSFETs and pn-diodes were prepared on such substrates (for details see ref.[8]). Electrical measurements of device parameters were carried out in the temperature range from 300 to 0.3 K. The defect structure was analyzed by applying a probe C_s corrected scanning transmission electron microscope (FEI Titan 80-300). Local strain fields are quantified by peak-pairs analysis (PPA) of high-resolution electron microscope images. Details of the measurements are described elsewhere.[7]

All simulations of the band structure and device simulations were performed using the GTS Framework simulation package,[9] enabling classical and quantum mechanical device simulations. For dislocations, the VSP tool within the simulation package was used representing a general-purpose device simulator for arbitrary nanostructures operating on the Schrödinger-Poisson equation system.[10]

COMMUNICATION

Well-defined sets of parallel dislocations, in the channel of metal-oxide semiconductor field-effect transistors (MOSFETs) result in a significant increase of the drain current (I_D). Figure 1 shows the transfer characteristics of nMOSFETs without and with dislocations in the channel. Devices without dislocations (reference) were prepared on identic SOI wafer without a dislocation network, in the 60 nm thick device layer and under the same process conditions. At a gate voltage $V_G = 0.8$ V and drain voltage $V_D = 0.4$ V, the drain current is about 40 μA for MOSFETs containing dislocations in the channel, while in the same time I_D is only 0.6 μA for a reference device. This corresponds to a current increase by a factor of 67. The increase of I_D depends on the type and number of dislocations in the channel. The increase in the drain current for nMOSFETs results from an increased electron transport along dislocations. On the other hand, an increase in I_D exists also for pMOSFETs, where holes are involved in the carrier transport along dislocations.[11] This means that depending on the properties of the surrounding material (p- or n-type) dislocations transport either electrons or holes.

Besides, I_D also the threshold voltage (V_T) and the sub-threshold swing of the MOSFETs dependent on the dislocation density.[12] Increasing, for instance, the number of dislocations by a factor of 10 results in a decrease of V_T from about −400 down to −150 mV. An explanation could be the dependence of V_T and the sub-threshold voltage shift (ΔV_T) on the effective channel length for MOSFETs.[13] Decreasing the effective channel length results in an increase of ΔV_T. If dislocations are present in the channel, the effective channel length is defined by the number of dislocations as the effective transport channels. Therefore, reducing the number of dislocations in the channel results in an increase of V_T and ΔV_T. On the other hand, the sub-threshold slope increases as the dislocation density increases. An analogous increase of the sub-threshold swing is generally interpreted as a thickness effect of the device layer for short channel SOI-MOSFETs and is caused by an inhomogeneous electron concentration in the layer.[14]

Measurements on individual defects (screw dislocations) proved a supermetallic behavior of dislocations caused by high strain levels inside dislocation cores.[7] The strain is uniaxial tensile along the dislocation line, that is, along <110>, and reaches about 10%, or more ($\varepsilon \approx +0.1$), which is much higher than the strain level induced by strained layers or other process-induced stressors. Calculations of the band structure result in quite significant alterations by such high strain levels.[11,15] A strain of $\varepsilon \approx +0.1$ causes shifts of the conduction and valence bands inducing smaller gaps but in different ways for tensile or compressive strain. Because of the small dimensions of the defects (diameter in the order of one nanometer, lengths up to a few micrometers), the band shifts make dislocations act as quantum wires. This interpretation was also confirmed by low-temperature investigations indicating the existence of an electron gas on dislocations. The existence of Shubnikov-de Haas oscillations refers to a two-dimensional electron gas for dislocation networks consisting of one-dimensional electron gases on individual dislocations. Furthermore, also single-electron transitions were obtained.[15,16]

Quantum mechanical device simulations proved the effect of strain-induced bandgap narrowing on the carrier transport along dislocations and the resulting interpretation of dislocations as quantum wires. Figure 2a shows schematically the model of an nMOSFET used for simulations. Without a dislocation in the center, the highest electron concentration exists close to the gate (Figure 2b). The silicon matrix (bulk) was assumed as p-type material with an acceptor concentration of 1×10^{15} cm^{-3}. Adding a dislocation into the center, the highest electron concentration appears at the defect (Figure 2c). The dislocation was assumed for the present simulation as n-type silicon having an electron (donor) concentration of 1×10^{18} cm^{-3}. A uniaxial tensile strain of $\varepsilon = +0.1$ (corresponding to a stress of $\sigma = 16$ GPa) in the dislocation was supposed. The confinement of carriers (electrons) on the dislocation is attributed to the strain-induced quantum wire formation. The electron concentration at the dislocation reaches $n_{el} = 3.5 \times 10^{19}$ cm^{-3} at $V_G = 0.7$ V and is, therefore, 35 times larger than the initial electron concentration assumed as 1×10^{18} cm^{-3} for the dislocation (Figure 2d). For the reference sample without a dislocation, the maximum electron concentration is observed close to the gate electrode. Similar values of n_{el} have been also obtained close to the gate for devices with dislocations, but they are significantly smaller than n_{el} at the dislocation. Figure 3a summarizes the effect of the gate voltage V_G on n_{el}. Increasing V_G increases n_{el} in both cases, but is much larger in devices containing a dislocation. At $V_G \geq 0.5$ V, the electron concentration is about a factor of 35 larger, if a dislocation is present. An increase of n_{el} by more than a factor of 10^4 results for MOSFETs with a dislocation in the channel at lower gate voltages ($V_G < 0.5$ V). The reason is the splitting into discrete energy levels in the quantum wire (a quantum well in the cross section). The effect depends on the diameter of the dislocation

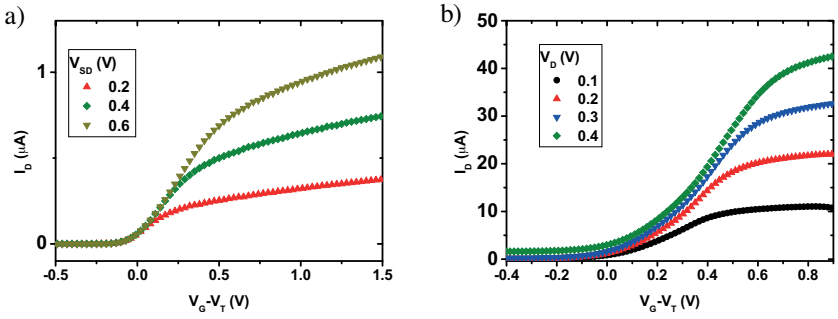

Fig 1. Transfer characteristics (I_D-V_G) of nMOSFETs without (a) and with dislocations in the channel (b). The gate voltage V_G is represented as difference V_G-V_{Th} with V_{Th} as threshold voltage. Note the different scale.

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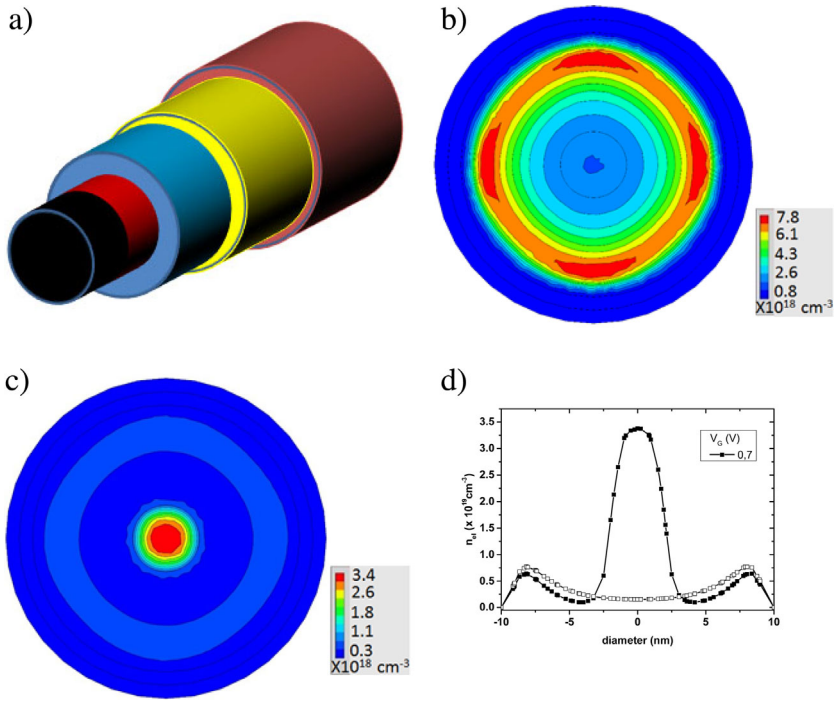

Fig 2. Model of a nMOSFET having a dislocation in the center (a). The dislocation (red, diameter 5 nm) is embedded in an unstrained silicon matrix (blue, diameter 20 nm) and surrounded by a thin gate oxide (yellow, 1 nm thick) and a gate electrode (brown). The source/drain contact on the dislocation is drawn in black. Cross-sections to the MOSFET showing the electron concentration at $V_G = 0.7$ V for a device without a dislocation (b) and with a dislocation in the center (c). The radial electron concentration is plotted in (d) for a device without (open symbols) and with a dislocation in the center (full symbols).

core representing the quantum wire. Increasing the diameter up to about 5 nm causes a significant increase of n_{el}. A further increase of the diameter yields that quantization effects will be more and more negligible and n_{el} is nearly constant. The strong increase even at low values of V_G refers to the shifts of the band structure and, therefore, with the number of energy levels inside the quantum wire.

The dominant effect of uniaxial strain in the dislocation core, shows Figure 3b. The electron concentration increases continuously with increasing strain, which is plotted in Figure 3b as stress $\sigma = E \cdot \varepsilon$ with E as Young's modulus ($E \cong 160$ GPa for uniaxial strain in <110>-direction[17]). The increase of n_{el} is a result of the increasing depth of the quantum well with increasing strain. This causes an increasing number of energy levels inside the well.

An initial electron concentration in the dislocation core of $N = 1 \times 10^{18}\,\mathrm{cm}^{-3}$ was assumed for all simulations. The reason for this value was a result of previously reported classical device simulations.[18] Here, the experimentally measured transfer characteristics were modeled with the electron concentration in the dislocation as fitting parameter. Quantum mechanical simulations, however, proved that the initial electron concentration is negligible. There are only small differences in n_{el}, if N is varied by more than two orders of magnitude (from 1×10^{16} to $1 \times 10^{18}\,\mathrm{cm}^{-3}$). This suggests that the enhanced carrier transport along dislocations is primarily not caused by an initially high electron concentration. Instead, the formation of the electron gas on dislocations is important. This results in the confinement of carriers and high carrier mobility. The impact of carrier mobility is the subject of further studies.

In summary, it is shown that a significant increase of the drain current exists if defined arrangements of dislocations are present in the channel of MOSFETs. Analyses of individual defects refer to a supermetallic behavior of dislocations. The reason is the extremely high strain in the dislocation core exceeding values of $\varepsilon \cong +0.1$. Such high strain causes substantial changes of the band structure and means that dislocations represent quantum wires. Quantum mechanical device simulations based on this conclusion, demonstrated

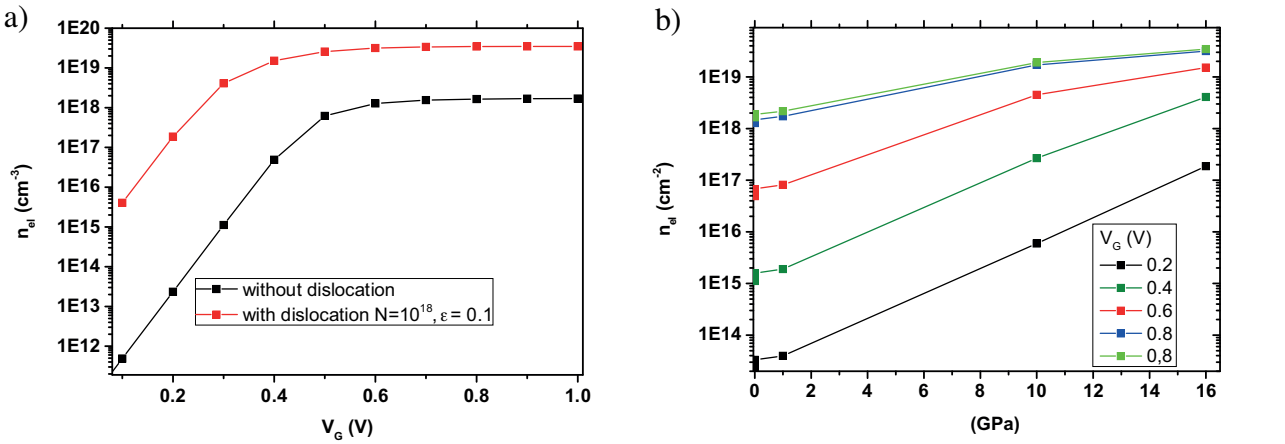

Fig 3. Calculated electron densities n_{el} for devices with and without a dislocation in the channel. Dependence of the electron density on V_G for a MOSFET with a dislocation in the center (dislocation diameter 5 nm, initial electron concentration $N = 10^{18}\,\mathrm{cm}^{-3}$, strain $\varepsilon = 0.1$) in comparison to devices without a dislocation (a). Dependence of n_{el} on the uniaxial tensile strain in the dislocation core at different gate voltages (b). The stress σ is plotted instead of strain for clearness.

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the transport of carriers on dislocations. The effect of gate voltage and strain in the dislocation core was analyzed in detail.

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[1] S. M. Sze, K. K. Ng, *Physics of Semiconductor Devices*, Wiley, Hoboken, **2007**.
[2] K. V. Ravi, *Imperfections and Impurities in Semiconductor Silicon*, Wiley, New York, **1981**.
[3] D. B. Holt, B. G. Yacobi, *Extended Defects in Semiconductors*, Cambridge University Press, Cambridge, **2007**.
[4] M. L. Polignano, I. Mica, G. P. Carnevale, A. Mauri, E. Bonera, S. Speranza, *ECS Trans*. **2012**, *50*, 303.
[5] M. Ieong, B. Doris, J. Kedzierski, M. Yang, *Science* **2004**, *306*, 2057.
[6] T. Skotnicki, *Microelectron. Eng*. **2007**, *84*, 1845.
[7] M. Reiche, M. Kittler, W. Erfurth, E. Pippel, K. Sklarek, *J. Appl. Phys*. **2014**, *115*, 194303.
[8] M. Reiche, M. Kittler, D. Buca, A. Hähnel, Q.-T. Zhao, S. Mantl, U. Gösele, *Jpn. J. Appl. Phys*. **2010**, *49*, 04DJ02-1.
[9] *Global TCAD Solutions GmbH*. **2016** Available from: www.gobaltcad.com.
[10] O. Baumgartner, Z. Stanojevic, K. Schnass, M. Karner, H. Kosina, *J. Comput. Electron*. **2013**, *12*, 701.
[11] M. Reiche, M. Kittler, E. Pippel, W. Erfurth, A. Haehnel, H. Uebensee, *Phys. State Solid C* **2015**, *12*, 1071.
[12] M. Reiche, M. Kittler, R. Scholz, A. Hähnel, T. Arguirov, *J. Phys. Conf. Ser.* **2011**, *281*, 012007-11.
[13] Z.-H. Liu, C. Hu, J.-H. Huang, T.-Y. Chan, M.-C. Jeng, P. K. Ko, Y. C. Cheng, *IEEE Trans. Electron. Dev.* **1993**, *40*, 86.
[14] E. Rauly, O. Potavin, F. Balestra, C. Raynaud, *Solid State Electron*. **1999**, *43*, 2033.
[15] M. Reiche, M. Kittler, H. Uebensee, E. Pippel, A. Haehnel, S. Birner, *Appl. Phys. A* **2016**, *122*, 389.
[16] M. Reiche, M. Kittler, M. Schmelz, R. Stolz, E. Pippel, H. Uebensee, M. Kermann, T. Ortlepp, *J. Phys. Conf. Ser.* **2014**, *568*, 052024.
[17] M. A. Hopcroft, D. Nix, T. W. Kenny, *J. Microelectromech. Syst*. **2010**, *19*, 229.
[18] M. Reiche, M. Kittler, M. Krause, H. Uebensee, *Phys. State Solid C* **2013**, *10*, 40.

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