Design and Optimization of Low Cost Booster-Based HF RFID Cards

Shrief Rizkalla, Member, IEEE, Ralph Prestros, and Christoph F. Mecklenbräuker, Senior Member, IEEE

Abstract—Novel designs for high frequency radio frequency identification cards comprise an intermediate circuit between the main coil and chip, such that the chip is not physically connected to the coil on card which reduces costs of production, enhances the card’s robustness against mechanical stress and improves communication capabilities. Based on the Bode–Fano limit, we carry out a theoretical analysis on the bandwidth capabilities of such types of cards and their derivatives. We verify these results through simulations and measurements of our own design, denoted as booster-based cards. An optimization method for the design parameters of the booster-based cards is presented and derived. Measurements on three booster-based card prototypes are carried out showing the various bandwidth and power capabilities of the cards. Additionally, a comparison between the performance of such type of cards with respect to the conventional ones is presented. Card measurements included a chip, highlighting various states of the chip and its non-linearity.

Index Terms—HF, RFID, coil, inductive coupling, booster, booster-based cards, chip, module, Bode-Fano, bandwidth, non-galvanic.

I. INTRODUCTION

The HF (High Frequency) RFID (Radio frequency identification) system has witnessed a significant growth in the market in the recent years. This is widely used in access cards for hotels, anti-theft techniques for shops, passport identification, contactless banking, transportation, disposable tickets…etc. The global RFID market has reached nearly 10 billion U.S. dollars where a significant challenge between different type of RFID systems exists. The HF RFID cards have been a focus of the research for the recent years in order to enhance their communication performance, reduce costs of manufacturing and provide better bandwidth, among other goals.

An HF RFID system operates at 13.56 MHz where it is composed of a reader (interrogator) which is power supplied and contains a coil in addition to a matching circuit to maximize its performance at the frequency of operation and provide different variants for possible data rates. ISO/IEC 10373-6 [1] provides a reference reader antenna design that is used for testing all contactless cards. A card, tested with this reference reader design, is assumed to operate properly with all ISO/IEC 14443 compliant readers.

The second part of the HF RFID system is the tag/card where we focus in our discussion on the passive tags, which means no power supply at the card side and communication is solely dependent on the power transmitted from the reader. They are conventionally composed of a coil that is connected to a chip with means of a physical connection, which we denote as galvanic connection. This galvanic connection jeopardizes the robustness of the card against mechanical stress and more importantly it increases the costs of manufacturing. In order to eliminate such connection, a “module” is utilized [2]. The module comprises the conventional RFID chip surrounded by a very small coil (module coil). The size of that coil is so small, that it fits in the area below the chip’s contact pads. Therefore, on its own the module can not achieve the same communication limits achieved by conventional HF RFID cards. Furthermore, a direct addition of a large coil covering the area of card and placing the module in a manner to achieve best possible coupling through this additional coil also does not reach the lowest limits defined by the standard for RFID cards, as shown in Section V. Therefore, there is a need for another circuitry in addition to the module to enhance the performance. In previous work, we have presented two alternative designs for such galvanic connection [3], [4]. In this work, we focus on presenting the general concept of such designs [5] in addition to discussing one of these two designs in a more thorough manner.

The paper is organized as follows: In Section II, a general design for non-galvanic cards is presented and the Bode-Fano limit is utilized to derive the bandwidth relation with respect to the card design. The booster-based cards are introduced in Section III where a circuit model and optimization criterion is presented. The derivations of the optimization criterion are available at the Appendix. We manufactured three prototypes based on the presented analysis to highlight various bandwidth capabilities of the booster-based cards. These prototypes in addition to a galvanic card design are discussed in Section IV. In Section V, the test setup is presented where a comparison between the three prototypes and galvanic card is carried out, in addition to measurements with a chip.

II. NON-GALVANIC DESIGNS

An RFID card operates within a weak coupling range with respect to the reader, where the coupling factor is in the range

2469-7281 © 2017 IEEE. Translations and content mining are permitted for academic research only. Personal use is also permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.
of 0.05. Therefore, one can study the card on its own without including the reader in order to simplify the analysis. A non-galvanic card would be composed mainly of a module and an additional circuitry. The module is composed of a chip and a small coil denoted as module’s coil. The module on its own cannot operate with the same performance level specified by the standard [1] because the module’s coil has a very small size that it cannot harvest enough power from the reader antenna. Therefore, an additional circuitry needs to be added in a manner that enhances the power transfer to the module. It is acceptable to assume that this additional circuitry would contain at least one coil, which is designed to cover the available area of the card/tag to enhance the coupling between the reader and the card. Since adding other elements within the additional circuitry would enhance the performance, we denote the remaining of the additional circuitry as “Circuit A”, for generality. Therefore, our system becomes as depicted in Fig. 1, where \( R_c \) and \( C_c \) are the simplified circuit model of the chip, \( L_m \) and \( R_m \) are the inductance and resistance of the module’s coil, and \( L_1 \) is the inductance of the additional coil. The parasitic capacitance of the module’s coil is combined with the chip capacitance \( C_c \). For simplicity, we do not consider in this analysis the parasitic capacitance and resistance of the additional coil. The voltage source and the source resistance (50 \( \Omega \)) in the figure are for theoretical purposes only, however, the card is passive and operates solely based on the magnetic field from the reader.

To adequately design the additional circuitry, one must define its requirements. The additional circuitry should efficiently transfer the power from the reader to the chip terminals. Since we have assumed that the additional circuitry is composed of at least one coil \( L_1 \), this coil must achieve that goal. Thus, it should cover a large area to maximize power harvested from the reader field and it should have a high coupling with respect to the module’s coil. This is simply achieved by dividing this inductance into two parts, one which is large to cover the tag/card area and a second small coil placed in close proximity to the module’s coil.

The next step is to study the structure of Circuit A and which elements should be included in it, in addition to understanding the effect of these elements on the operation of the card. One of the main aspects that receives much attention is the bandwidth of the card. We analyze the bandwidth capabilities of the card using the Bode-Fano limit. This limit is studied for a circuit composed of a matching circuit and a shunt RC load.

Thus, to utilize such limit we express the circuit in previous figure as shown in Fig. 2, where we utilize the 3 T-shaped inductances to include the mutual coupling \( M \) between the coils \( L_1 \) and \( L_m \). Thus, the matching circuit as in Bode-Fano limit is here composed of circuit A, the 3 T-shaped inductances and resistance \( R_m \).

The quality factor - bandwidth limit, for a circuit as in Fig. 2 composed of a matching circuit and a shunt RC load, is known as the Bode-Fano criterion [6], [7] and is given by

\[
\int_0^\infty \ln \left| \frac{1}{\Gamma} \right| \, d\omega \leq \frac{\pi}{R_c C_c},
\]

(1)

where \( \Gamma \) is the reflection coefficient of the matching circuit measured from the source side. Bode [6] was first to derive the theoretical relationship for the relative bandwidth \( B_{\infty} \) using a matching circuit composed of an infinite number of elements [8]. For that case, we assume ideal matching conditions such that \( \Gamma_m \) is the minimum reflection coefficient which is constant over the frequency band \( f_1 \) to \( f_2 \). Therefore,

\[
\int_{\omega_1}^{\omega_2} \ln \left| \frac{1}{\Gamma_m} \right| \, d\omega = (\omega_2 - \omega_1) \ln \left( \frac{1}{\Gamma_m} \right) = \frac{\pi}{R_c C_c}.
\]

(2)

Hence, this equation is interpretable as

\[
QB_{\infty} = \frac{\pi}{\ln \left( \frac{1}{\Gamma_m} \right)},
\]

(3)

where \( Q = \omega_c R_c C_c \) is the quality factor of the load, \( B_{\infty} \) is the relative bandwidth which is the bandwidth divided by the operating (center) frequency \( \omega_c \) and the subscript \( \infty \) refers to the order of the matching circuit. Based on this equation, we interpret that for a certain load, the ratio of the bandwidth and reflection coefficient is constant. Thus, increasing the bandwidth is opposed by a change in the reflection coefficient. Applying that equation to our HF RFID card, we deduce that there is a trade-off between the bandwidth and the amount of voltage transferred to the chip (can be expressed in terms of the usable distance between reader and card).

Fano [7] has determined the quality factor - bandwidth limit for any order \( n \) of the matching network, where the order of the matching network is defined by the number of resonant frequencies in the whole circuit. Lopez [9] provided a simplified expression for the quality factor - bandwidth product \( QB_n \) using

\[
QB_n = \frac{1}{b_n \sinh \left( \frac{1}{\omega_c} \ln \left( \frac{1}{\Gamma} \right) \right) + \frac{1 - b_n}{\omega_c} \ln \left( \frac{1}{\Gamma} \right)},
\]

(4)
where $a_n$ and $b_n$ are constants calculated by Fano and enhanced in [9]. Fig. 3 shows the results of the quality factor - bandwidth product versus the reflection coefficient for different matching circuit orders.

Lopez [9] has also calculated the percentage of bandwidth increase for $\Gamma > 0.33$ with respect to changing the order of the matching circuit as depicted in Fig. 4. One observes that the highest gain in bandwidth is achieved at order 2 which leads to 100% increase in bandwidth. However, for higher orders the increase in bandwidth is nearly 20% or less which does not seem to pay off.

III. Booster-Based Cards

Reviewing the previous results and the amount of bandwidth gain resulting from incrementing the order of the matching network, we reach the conclusion that a matching circuit with order 2 provides the best compromise between utilized bandwidth and circuit complexity. The circuit complexity increases significantly by adding elements to the matching network, as one would end up with at least 7 variables for a circuit of order 2 and then all these variables needs to be optimized to reach the optimum solution that maximizes power transfer from reader to card while taking into account the bandwidth capabilities. Thus, we focus in the next parts of this work on adding a matching circuit with order 2 to an RFID card using a module. A circuit with order 2 means that we should end up with 2 resonance frequencies on our card, which means in addition to the module’s coil, we can add a capacitor and an inductor to our circuit.

Identifying the purpose of the coil on the matching circuit would help determining its design. The coil should be able to harvest as much power possible from the reader, therefore, it needs to cover the whole available area of the card. On the other side, the coil should be strongly coupled to the module’s coil such that it can efficiently transfer the harvested power to the chip. Thus, we separate that coil into two; one covering the large perimeter of the card and the other would be a small coil placed at a close proximity to the module. Furthermore, to reach a matching circuit with order 2, we need to add another capacitor where there are 2 possibilities; either adding it in parallel or series to the coils of the matching network. The properties of a parallel LC circuit show that the circuit would have high resistance at resonance which would not be useful for our circuit. Thus, we place the capacitor in series with the two coils. The design of the matching circuit without the module’s coil is depicted in Fig. 5, where we denote primary, secondary coils and capacitor as a booster [10]. The points “1” and “2” marked in blue on the figure are to be connected with a different layer. In such design, the module is placed directly on top of the secondary coil, ensuring highest coupling coefficient between module’s coil and secondary coil.

Simulating such a design can be achieved through the use of 3D electromagnetic field simulator such as HFSS. This provides accurate results at the expense of high complexity and high simulation time. Determining the circuit model for such a card leads to achieving a more robust method for designing such cards. In Fig. 6, we introduce our circuit model of the booster-based cards. A spiral coil is modeled through a series resistance and inductance in addition to a parallel capacitance. The capacitance of the module’s coil is combined with the chip capacitance $C_C$ for simplicity. The capacitor $C_B$ is the lumped capacitor in the booster.

In order to optimize such a circuit, we first list some simplifications; The capacitance of the secondary coil $C_2$ is usually a very small value $\approx 0.7$ pF, so it is fine to ignore it, as that
would simplify the analysis. The resistances of primary and secondary coils are simplified, combined and expressed as $R_B$. We also identify several coupling coefficients in the system, however, for the current analysis of the card only, the dominant coupling between $L_2$ and $L_m$ is considered and denoted by $M$. We utilize the 3 T-shaped inductances $L_2 - M$, $L_m - M$ and $M$ as in Fig. 7 to include the mutual inductance in our circuit.

Assuming we have a certain chip load, we determine the matching circuit elements. The dominant elements that require optimization are highlighted in red in Fig. 7.

We have two resonance frequencies in the booster-based cards; one from the module and the second from the booster (there are more resonant frequencies rising due to the coils’ parasitic capacitance, however, they are far from the frequency of operation, so they are not relevant). An optimization criterion is defined ensuring that both dominant resonance frequencies are close around the frequency of operation. This optimizes the power transfer characteristics and resulting bandwidth. Through some lengthy derivations, we are able to calculate the real and imaginary parts of the total impedance $Z_t$ for the circuit in Fig. 7. The condition for resonance is that the imaginary part should be equal to zero at the frequency of operation. Based on our derivations, we present our optimization steps which maximizes power transfer at frequency of operation, where derivations are available in the Appendix. First, we choose the module inductance such that

$$L_m = \frac{R_c^2 C_c}{1 + \omega^2 R_c^2 C_c}$$  

where $\omega_o$ is the frequency of operation in radians per second.

The choice of the secondary coil is left as a free element for the designer to decide, as it is useful to control the bandwidth of the card as will be shown later. We recommend keeping it small (nearly 1 $\mu$H), such that it has high mutual inductance to the module’s coil and also allowing the primary coil to be large enough to maximize energy harvested from the reader coil. The choice of the booster capacitor has a direct impact on the bandwidth of the card and higher is better. However, the capacitance value is usually upper bounded by the industrial capabilities. The inductance of the primary coil is chosen according to

$$L_1 = \frac{1 - \omega_o^2 L_2 C_B}{\omega_o^2 C_B + \omega_o^4 C_1 - \omega_o^4 L_2 C_1 C_B}$$  

The final element is the mutual inductance between the secondary coil and module’s coil. This element affects the bandwidth of the card at the expense of the delivered power. Therefore, it should be chosen according the application and the design requirements whether it is distance or bandwidth oriented. Controlling the mutual inductance is achieved by the choice of the dimensions of the secondary coil, since the module’s coil is placed on top of the secondary coil. The higher the mutual inductance is, the more bandwidth the card realizes.

The strength of the coupling is categorized in literature into 3 stages: under-, critical- and over-coupling [11], as depicted in Fig. 8. The under-coupled state occurs when the coupling coefficient is below a certain critical value and is characterized by a low gain (transfer function). Critical coupling is the optimum coupling value delivering highest power transfer with one peak at the resonance frequency. Lastly, the over-coupled state is characterized by two peaks in the power transfer function with a small ripple where the local minimum occurs at the resonance frequency, however, its advantage is covering a larger bandwidth. The critical coupling factor for a double tuned circuit, as our booster-based card, is given by

$$K_{BM-c} = \frac{1}{\sqrt{Q_{Booster} Q_{Module}}}$$  

where $Q_{Booster} = \frac{1}{w_0 R_B C_B}$ and $Q_{Module} = w_0 R_c C_c$ are the quality factor of the booster and module, respectively [12], [13]. Therefore, the critical coupling factor for the booster-based cards is

$$K_{BM-c} = \frac{R_B C_B}{R_c C_c}.$$
It is noted that the coupling here refers to the coupling between the booster \( (L_1 + L_2) \) and the module’s coil \( L_m \), hence, the subscript \( BM \). Thus, if the card is to be designed for maximum read range, regardless the bandwidth, the designer targets a coupling as close as feasible to the critical coupling factor \( K_{BM} \).

### IV. Prototypes

In this section, we utilize the previous analysis to create booster-based prototypes. We consider an NXP chip with nominal capacitance 69 pF and resistance 1850 \( \Omega \) as specified by the manufacturer. In reality, the chip is much more complex and its behavior varies according to the applied voltage [14]. However, for the current analysis we consider this simplified model. First, we choose the inductance of module’s coil using (5) which gives \( L_m = 2.03 \) \( \mu H \). A module’s coil is limited by the dimensions of the module which is \( 11.4 \times 12.6 \) mm. Using FastHenry simulation [15], we determine the dimensions of the coil which result in the target inductance, considering the manufacturing capabilities. We choose an 0.7 \( \mu H \) inductance for the secondary coil. In order to highlight the effect of the mutual inductance on bandwidth, we create variants of this secondary coil to reach different mutual inductances \( M \) between the module’s coil and secondary coil. The booster capacitor is chosen to be 22 pF. The inductance of the primary coil is calculated by (6) which results \( L_1 = 4.7 \) \( \mu H \).

Through the use of FastHenry, we choose the proper geometries for the first card, denoted by “Card 1” that correspond to the previously calculated values, as indicated in Table I. The variable ‘N’ indicates the number of turns, ‘a’ and ‘b’ are the width and length of the coil, respectively. The track width and height are given by ‘w’ and ‘h’, and ‘g’ is the gap between two adjacent wires. After determining the dimensions of the coils, the assumed values of the parasitic elements \( (C_1, R_m, \ldots) \) can be calculated and reused in (5) and (6). This iteration is repeated a couple of times for higher accuracy. Furthermore, we manufacture two more cards where the only difference is in the dimensions of the secondary coil. It is noted that the inductance value is still the same 0.7 \( \mu H \), however, we use different dimensions in order to increase the mutual inductance \( M \) to the module’s coil. Table II, shows the dimension of the secondary coil for “Card 2” and “Card 3”.

We also identify that the system becomes more complex with more mutual inductances between the reader, booster-based card and also within card itself. The two dominant coupling coefficients are between the reader and primary coils and that between the secondary and module’s coils. There are 3 more mutual inductances which have low effect.

We present in Table III all the mutual inductances for Card 1 which is separated by a distance of 37.5 mm from the reader.

For the purpose of testing, we carry out several measurements with a known load instead of the chip. Thus, we have soldered a lumped RC load on a module, with \( R_c = 1800 \) \( \Omega \) and \( C_c = 68 \) pF which are the closest standard values for the assumed load of the chip. Fig. 9 shows the three manufactured prototypes for booster-based cards with different secondary coil dimensions. The module with a chip can be seen in Fig. 9(a) and the second module with RC equivalent load is in Fig. 9(b). It is noted that we utilize modules without contact pads in order to simplify the analysis, where the contact pads shift the resonance frequency of the module slightly. We have previously investigated booster-based cards with modules with contact pads in [3].

To create a comparison to the normal galvanic cards, we designed a coil for direct connection to a 69 pF chip. The card is composed of one coil with the dimensions of \( 50 \times 80 \) mm, 3 turns, \( 0.3 \) mm track width, \( 0.3 \) mm gap and \( 0.035 \) mm track height. This card is denoted as “Galvanic Card” and is shown in Fig. 10. We have two prototypes; one with a chip and the second with a lumped RC load. For a fair comparison, we used an identical chip as in the modules. On the manufactured galvanic cards, there are 2 pins which are placed only for connecting the measurement.


### Table I

Dimensions of the Primary, Secondary and Module’s Coils for “Card 1” (All Values are in mm Units)

<table>
<thead>
<tr>
<th>Primary</th>
<th>Secondary</th>
<th>Module</th>
</tr>
</thead>
<tbody>
<tr>
<td>N w h</td>
<td>w h</td>
<td>a</td>
</tr>
<tr>
<td>a 80.5 g 0.3 b 50 h 0.035</td>
<td>a 21 g 0.3 b 21 h 0.035</td>
<td>a 11.4 g 0.025 b 12.6 h 0.018</td>
</tr>
</tbody>
</table>

### Table II

Dimensions of the Secondary Coils for Cards 2 and 3 (All Values are in mm Units)

<table>
<thead>
<tr>
<th>Card 2</th>
<th>Card 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>N w h</td>
<td>N w h</td>
</tr>
<tr>
<td>a 17.5 g 0.3 b 17 h 0.035</td>
<td>a 15 g 0.3 b 16 h 0.035</td>
</tr>
</tbody>
</table>

### Table III

The Mutual Inductances Between the Reader Antenna and Card 1

<table>
<thead>
<tr>
<th>Primary</th>
<th>Secondary</th>
<th>Module</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reader</td>
<td>Secondary</td>
<td>Module</td>
</tr>
<tr>
<td>100 nH</td>
<td>5 nH</td>
<td>6 nH</td>
</tr>
<tr>
<td>Module</td>
<td>80 nH</td>
<td>( M = 310 ) nH</td>
</tr>
</tbody>
</table>
Fig. 10. Manufactured galvanic card with (a) a 69 pF chip (b) a lumped RC load.

### TABLE IV

<table>
<thead>
<tr>
<th>Primary</th>
<th>Secondary</th>
<th>Module</th>
<th>Booster and chip</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_1$ 4.7 µH</td>
<td>$L_2$ 0.7 µH</td>
<td>$L_m$ 2.1 µH</td>
<td>$C_B$ 22 pF</td>
</tr>
<tr>
<td>$R_1$ 3 Ω</td>
<td>$R_2$ 0.7 Ω</td>
<td>$R_m$ 5.4 Ω</td>
<td>$R_c$ 1800 Ω</td>
</tr>
<tr>
<td>$C_1$ 49 pF</td>
<td>$C_2$ 1 pF</td>
<td>$C_m$ 2 pF</td>
<td>$C_e$ 68 pF</td>
</tr>
</tbody>
</table>

Through utilizing FastHenry and HFSS, we calculate the value of the circuit elements in Fig. 6. Table IV shows the values of all circuit elements for Card 1. For Card 2 and Card 3, the only difference is in the secondary coil. We have manufactured it to have an inductance of nearly 0.7 µH and there is not a significant change in the parasitic elements also. However, the mutual inductance between the secondary coil and the reader are changed where for Card 2, it is equal to 0.64 µH. Since the secondary coil of Card 3 has more turns directly below the module’s coil, it has the highest mutual inductance $M = 0.94$ µH.

### V. TEST SETUP AND RESULTS

In order to achieve practical results for the operation of our booster-based cards in an actual RFID system, we include the reader into our setup. The reference reader coil is specified at the ISO/IEC 10373-6, where we use test Proximity Coupling Device (PCD) layout 1 (available at Annex A [1]) for both simulations and measurements. The standard defines a measurement setup composed of a Test PCD assembly where the reader coil and card are separated by distance of 37.5 mm. We utilize this setup in Fig. 11 which is composed of a reader coil connected to a signal generator (R&S SMU 200A). The card under test is placed on the test PCD assembly and an active probe is used to measure the voltage transferred from the reader to the terminals of the chip or lumped load. In such a setup, it is essential to use an active probe rather than a normal passive probe, since the parasitic capacitance of such probes is very low (~1 pF) in contrast to a (~10 pF) capacitance for passive probes. Such high capacitance value would be relatively close to the capacitance of the chip which means it would detune the results [16]. The active probe (R&S RT-ZD30) is connected to a signal analyzer (R&S FSQ26) in order to visualize the results.

A computer is used to control the center frequency of both the signal analyzer and generator simultaneously, in order to carry out a frequency sweep. Fig. 12 shows the test setup at our lab, where the Test PCD Assembly is shown on the right and the card is placed on top. The reader is placed in the second slot at the distance 37.5 mm. The second sense coil is located at the last slot which is placed in accordance to the standard, but does not influence the measurements in our setup.

We also carried out a 3D electromagnetic field simulation using HFSS for the whole system including the reader coil. Fig. 13 shows our simulation structure at HFSS, where we consider the same distance between reader and card. The reader is implemented exactly as specified by the standard and the card is modeled including the substrate of the PCB (FR4 epoxy) and that of the module (epoxy glass). The corresponding circuit model of this system is simulated using ADS, where the reader circuit model is available at the standard [1]. For the card, the circuit model in Fig. 6 is used along with the values from Table IV.

We compare the results of our simulations and measurements for Card 1 in Fig. 14, where a 10 dBm power is used
at the reader coil. For the results in this figure, we used the module containing the lumped RC load. This helps identify the behavior of the card without the effect of the chip’s non-linearity. The results show that our optimization criterion achieved its goals successfully, where the voltage transfer is optimized around the frequency of operation (13.56 MHz) without having any peaks at higher frequencies. We also measure the voltage transferred for Card 1 without the booster capacitor $C_B$, where we observe that the peak of the voltage transferred is almost 0.06 V against 1.6 V for our booster-based design, as shown by the magenta curve. Our design with the capacitor enhances the voltage transfer by nearly 30 dB $[10]$. It should be noted that the current coil dimensions might not be the optimum one for a card without the booster capacitance $C_B$, however, proper tuning of the dimensions would still keep the voltage within the same range. Furthermore, the circuit simulations by ADS and electromagnetic simulations by HFSS show an agreement with the measurements which confirms the accuracy of our proposed circuit model and the calculated values. HFSS simulation has a slight shift in frequency in comparison to the circuit simulation and measurements. This is due to including all details of the reader and card which makes the field simulation more complex.

As mentioned in Section III, changing the mutual inductance $M$ between the secondary and module’s coils affects the bandwidth of the card. Thus, we verify this claim through the three booster-based prototype cards, where each of them has different dimension for the secondary coil which means different mutual inductance, yet they still have the same inductance value $L_2$. According to design, Card 1 should have lowest mutual inductance, therefore smallest bandwidth, while Card 3 would have the biggest bandwidth among the three cards.

Fig. 15 shows the results of measuring the voltage transferred to the terminals of the lumped load on the module for the booster-based prototypes in addition to the galvanic card. We observe that the three cards have different bandwidths where bandwidth is defined by the 3dB bandwidth from the peak of the transferred voltage, which means the region where the voltage drops by $\sqrt{2}$ from the maximum. Card 1 has 1.9 MHz bandwidth, Card 2 reaches 3.1 MHz and Card 3 achieves the largest bandwidth of 4 MHz, where all cards have nearly a center frequency around 13.4 MHz. This is aligned with our optimization criterion previously discussed.

Furthermore, we relate these results with the Bode-Fano limit expressed by Fig. 3, where the Bode-Fano limit states that as the return loss increases, the bandwidth decreases. This is observed here in Fig. 15, where as the bandwidth increases, the maximum voltage that the card reaches, is decreased. Moreover, to link these curves with the degree of coupling shown before at Fig. 8, the critical coupling factor for such card is $K_{BM-c} = 0.025$, according to equation (8). The coupling factor between the booster and module for the three booster-based cards are $K_{BM}^{Card\ 1} = 0.09$, $K_{BM}^{Card\ 2} = 0.19$ and $K_{BM}^{Card\ 3} = 0.28$. Thus, we observe that Card 1 shows a beginning of over-coupling behavior where its voltage is relatively close to the optimum and bandwidth is slightly enhanced. For Cards 2 and 3, the over-coupling behavior is obvious where we note the two peaks and lower voltage level.
Based on Fig. 15, the booster-based cards achieve several advantages over the galvanic cards at the expense of higher complexity. Firstly, the main goal of removing the galvanic connection between the main coil and chip is satisfied, which enhances card’s robustness against mechanical stress and reduces costs of production. Through comparing the voltage delivered to Card 1 with that from the galvanic card, we have reached nearly the same level (difference of 6%). On the other side, the booster-based Card 1 is able to achieve higher bandwidth of 1.9 MHz in comparison to 1.5 MHz for the galvanic card. Different variants of the booster-based cards (Cards 2 and 3 and other possible structures) can achieve higher bandwidths for the same chip load. This flexibility is not available for normal galvanic cards, as there exists only one coil which has to be tuned to the 13.56 MHz, thus rendering the same bandwidth no matter the dimensions of the coil (if correctly tuned at 13.56 MHz). As presented here, we were able to achieve different bandwidths (up to 4 MHz) for the same chip load by changing the dimensions of the secondary coil on the booster.

After analyzing the behavior of the booster-based cards, we replace the lumped load with an actual chip, using the module shown in Fig. 9(a). Since the chip’s behavior is dependent on the delivered voltage, we sweep the reader’s power starting from 0 dBm up to 24 dBm and we show in Fig. 16 the results for the galvanic card and booster-based Card 3. Thus, we expect that the galvanic card would have a higher voltage but lower bandwidth with respect to the booster-based card. The chip’s behavior has been investigated where different blocks of analog and digital circuits operate within the chip dependent on the voltage at its terminals [14,17]. At low voltage, the chip exhibits a relatively high resistive value (≈3KΩ) and as the voltage increases, the value of the resistance is decremented [14]. The chip enters a power-on reset state at an RMS voltage of nearly 1.5 V, where at this point the chip starts setting some of its blocks to a predefined state. The resistance of the chip at that state exhibits two spikes at nearly 1 and 1.5 V. We can observe these spikes at 6 and 12 dBm curves of the galvanic card. Up till the 12 dBm power, the chip has not started operating yet and we can observe that the galvanic card achieves higher voltage and lower bandwidth compared to booster-based ones as expected. The Controller Processing Unit (CPU) of the chip is set to start operating at nearly 2 V [14]. After this point, the slope of chip’s resistance change is reduced, which means the reduction in chip’s resistance is less with respect to the applied voltage. For the galvanic card, we notice the power-on reset spikes for 18 dBm at nearly 12 and 15 MHz and the spike of the start of operation of the chip at nearly 12.5 MHz. For higher power, we observe that the booster-based card achieves nearly the same voltage as the galvanic one and even outperforms it, while having higher bandwidth capabilities. The behavior of the booster-based cards is more sensitive to the change in chip’s load, as can be depicted by the unsymmetrical behavior around the chip’s operating state (18 dBm) which is expected as the circuit is more complicated, as a result it would behave differently to the galvanic card. However, it is still operating within the acceptable range, as the fluctuations in the voltage are not severe. It is noted that the standard ISO/IEC 14443 [18] states that the card should be able to communicate at a minimum field intensity of 1.5 A/m. This means that at that field intensity, the chip should reach at least 2 V. The booster-based cards were able to achieve such limit, where the chip starts operating at an input power of 18 dBm which is equivalent to nearly 0.4 A/m.

VI. Conclusion

We present a novel design which enhances the robustness of the card against mechanical stress and reduces its cost of production while preserving the quality of communication. Through utilizing the Bode-Fano limit, the bandwidth gain of the card versus the added complexity is investigated. We conclude that a matching circuit of order 2 provides the best compromise between bandwidth and complexity. We introduced a circuit model for the booster-based cards and deduced theoretical derivations in order to optimize the voltage transfer to the card. The optimization shows a method to determine the values of 5 dominant elements within the card, while considering the parasitic elements. Three booster-based prototypes were manufactured that achieve different bandwidth capabilities based on the dimension of the secondary coil. This is also the first work to compare the behavior of such cards to a galvanic card where we found that the booster-based cards have more advantages in terms of bandwidth control for a certain chip load. Thus, providing more flexibility over the galvanic cards while not sacrificing the amplitude of the transferred voltage. HFSS and circuit simulations are carried out for a card with a lumped load and compared to measurements where the results are in a good alignment confirming our proposed circuit model. We have also measured the behavior of the card with a chip while considering different input powers. The booster-based cards show a slightly more complex and sometimes non-symmetric behavior during the chip transition states, however, their behavior is in the same range as that from the galvanic card while achieving more bandwidth.
APPENDIX

In this section, we list the derived equations for real and imaginary impedance of the circuit given by Fig. 7. Although, the expressions are lengthy, they are merely calculated through substitution of variables, so these calculations are not computationally expensive. The real part of the card’s impedance is expressed by

\[
Re(Z_T) = R_B + \left[ w^2 R_m M_1^2 + w^2 R_m M_2^2 + w^4 R_m^3 M_1^2 C_c^2 + 2 w^4 R_m^2 M_1^2 C_c^2 + w^6 R_m^3 M_2^2 C_c^2 \right] /
\]

\[
\left[ \left( R_m + R_c + w^2 R_m^2 R_c C_c^2 \right)^2 + \left( -w R_c^2 C_c + w L_m + w^3 L_m R_c^2 C_c^2 \right)^2 \right]
\]

(9)

Assuming that \( Re(Z_T) = r \), where \( r \) is an arbitrary real value, we rearrange the equation in terms of \( L_m \), such that

\[
L_m^2 \left( w^2 r + w^6 R_c^2 C_c^2 + 2 w^4 R_c^2 C_c^2 \right)
\]

\[
+ L_m \left( -2 w^4 R_c^2 C_c^2 - 2 w^2 R_c^2 C_c \right)
\]

\[
+ \left( R_c^2 r + R_m^2 r + w^4 R_m^2 R_c C_c^2 + 2 w^2 R_m^2 R_c C_c^2 \right)
\]

\[
- w^2 M_1^2 R_c - w^2 M_2^2 R_m - 2 w^4 M_2^2 R_c^2 C_c^2
\]

\[
- w^4 M_1^2 R_c C_c^2 - w^6 M_2^2 R_m^2 C_c^2 \right) = 0
\]

(10)

From this equation, one can deduce that there are two values of \( L_m \) that can satisfy this equation at a certain frequency and resistance \( r \). Based on the knowledge that this is a resonant circuit which would have a maximum resistance value at only one point, we need to find the unique value of \( L_m \) which satisfies that condition. Since this is a quadratic function in the form \( ax^2 + bx + c \), there is one unique solution when \( x = -b/2a \). Applying the same approach on the equation, we reach that

\[
L_m = \frac{R_c^2 C_c + w^2 R_c^3 C_c^3}{1 + w^4 R_c^2 C_c^3 / 2 w^2 R_c^2 C_c^3}
\]

(11)

where \( w_c \) is the frequency of operation in radians per second. After eliminating the equal terms from numerator and denominator, the module inductance is expressed by

\[
L_m = \frac{R_c^2 C_c}{1 + w^2 R_c^2 C_c^3}
\]

(12)

This equation can also be interpreted by considering the imaginary part of the impedance (13), where choosing \( L_m \) according to the previous equation makes the imaginary impedance independent of the reactive elements in the module side. In other words, the imaginary impedance at the module circuit becomes zero at the frequency of operation.

The imaginary part of the total impedance is expressed by

\[
Im(Z_T) = \frac{w L_1}{1 - w^2 L_1 C_1} - \frac{1}{w C_B} + w L_2
\]

\[
+ \left[ w^3 M_2 \left( -L_m - 2 w^2 M_2 R_c^2 C_c^2 + R_c C_c \right) - w^4 L_m R_c^2 C_c^2 + w^4 R_c^2 C_c^2 \right] /
\]

\[
\left[ \left( R_c + R_c + w^2 R_m^2 R_c C_c^2 \right)^2 + \left( -w R_c^2 C_c + w L_m + w^3 L_m R_c^2 C_c^2 \right)^2 \right]
\]

(13)

It can be simplified, using the previous condition on \( L_m \), at \( w = w_c \), such that

\[
Im(Z_T) = \frac{w L_1}{1 - w^2 L_1 C_1} - \frac{1}{w C_B} + w L_2.
\]

Therefore, to achieve resonance, the primary coil has to be calculated according to

\[
L_1 = \frac{1 - \omega_c^2 L_2 C_B}{\omega_c^2 C_B + \omega_c^2 C_1 - \omega_c^2 L_2 C_1 C_B}.
\]

(15)

ACKNOWLEDGMENT

The authors would like to thank Alexey Nazarov and his team for manufacturing the prototypes presented in this work.

REFERENCES


Shrief Rizkalla received the bachelor’s degree (Distinction with Hons.) in electronics and communication engineering from Ain Shams University, Cairo, Egypt, in 2011, and the master’s degree (with Distinction) in communications technology program from Ulm University, Germany. He is currently pursuing the Ph.D. degree with the Institute of Telecommunications, Technische Universität Wien, Vienna, Austria.

He was with the “Near Field Power Efficiency” project, the Christian Doppler Laboratory for sustainable mobility from 2014 to 2016. Since 2014, he has been a Research Assistant with the Institute of Telecommunications, Technische Universität Wien. He is currently involved in the “Advanced Inductive Coupling” project in cooperation with NXP Semiconductors GmbH. His research interests include RFID, antenna’s design, compressed sensing, and channel coding. He was a recipient of the Best Paper Award at Loughborough Antennas and Propagation Conference (LAPC 2016) for his paper on coupling frame-based HF RFID Cards, and a recipient of the Best Student Award and was awarded for his master’s thesis on channel coding and compressed sensing by VDE for best thesis with Ulm University.

Ralph Prestros received the M.Sc. degree (with Distinction) in electrical engineering from the Technical University of Vienna, Austria, in 2003. Until 2008, he was with Infineon Technologies on contactless smart-card testing and represented Infineon and Austria in various international standardization bodies. In 2008, he joined the Application Engineering Team for identification products with NXP Semiconductors, where he has been supporting customer in improving their RFID antenna design as well as in EMC and EMI optimization.

Christoph F. Mecklenbräuker received the Dipl.-Ing. degree (with Distinction) in electrical engineering from Technische Universität Wien, Vienna, Austria, in 1992, and the Dr.-Ing. degree (with Distinction) from Ruhr-Universität Bochum, Bochum, Germany, in 1998. He was a recipient of the Gert-Masenberg Prize for his doctoral dissertation on matched field processing in 1998.

From 1997 to 2000, he was with Siemens, Vienna. He was a delegate to the Third-Generation Partnership Project and engaged in the standardization of the Universal Mobile Telecommunications System. From 2000 to 2006, he held a Senior Research position with the Forschungszentrum Telekommunikation Wien, Vienna, in the field of mobile communications. In 2006, he joined the Faculty of Electrical Engineering and Information Technology as a Full Professor with the Technische Universität Wien, Vienna. From 2009 to 2016, he has led the Christian Doppler Laboratory for Wireless Technologies for Sustainable Mobility. He has authored approximately 100 papers in international journals and conferences, for which he has also served as a reviewer, and holds eight patents in the field of mobile cellular networks. His current research interests include vehicular connectivity, ultra-wideband radio, and multiple-input multiple-output techniques for wireless systems.

He is a member of the IEEE Signal Processing, Antennas and Propagation, and Vehicular Technology Societies as well as the Association for Electrical, Electronic and Information Technologies e. V. and the European Association for Signal Processing.