# Influence of Boron Antisite Defects on the Electrical Properties of MBE-Grown GaAs Nanowires

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**Nanowires provide a platform for the integration of heterogeneous materials in III–V systems grown on Si. $B_xGa_{1-x}As$ is an interesting material for strain applications, which has not yet been studied in nanowire form. The incorporation of boron in GaAs nanowires is investigated via DC-IV measurements. In transmission electron microscopy analysis a high concentration of boron is found at the nanowire edges, indicating surface segregation during growth. Nanowires grown under boron flux are found to exhibit Ohmic contacts and low contact resistances with p-type metallizations such as Au/Zn/Au or Cr/Au. Back-gated measurements confirmed the p-type behavior of such nanowires, indicating that boron is incorporated on antisite defects where it acts as a doubly-charged acceptor. This offers a new route for the inclusion of p-doped layers in GaAs-based nanowire heterostructures and the subsequent formation of Ohmic contacts.**

## 1. Introduction

The growth of the ternary material $B_xGa_{1-x}As$ has been sparsely investigated, despite potential applications in strain engineering and optoelectronics.[1,2] In planar growth, the material is interesting for strain compensation in the growth of $GaAs/In_xGa_{1-x}As$ heterostructures.[3] There are several well-documented problems in the molecular beam epitaxy (MBE) growth & characterization of planar $B_xGa_{1-x}As$, such as surface segregation, rough surface morphologies, and a high density of antisite defects.[4,5]

Nanowire (NW) growth of B:GaAs allows for further investigation into the growth kinetics of this ternary material, as well as for the possible incorporation in NW heterostructures. Due to the small lattice constant of BAs (4.76Å,[6]), the addition of small amounts of boron to GaAs can lead to strain in NWs with minimal change to the bandgap. This allows for strain compensation in NW heterostructures containing $In_xGa_{1-x}As$.[7,8]

In addition, since $B_{As}$ acts as a doubly charged acceptor,[9] incorporation of boron in planar GaAs layers was found to lead to high unintentional p-doping.[10,4] This offers an alternative route to p-doping in MBE-grown GaAs nanowires than those previously demonstrated, which include Be[11] or Si.[12,13] One interesting aspect of using B to dope GaAs nanowires is that since it is group III, it offers the possibility to tune the growth parameters between substitional incorporation or incorporation on defect sites.

The addition of boron during growth of GaAs nanowires (NWs) leads to growth of a B:GaAs shell displaying many of the properties described for layer growth (such as a rough surface and a high concentration of boron at the surface suggesting segregation).[14] In this article we will explore the electrical characteristics of these NWs and discuss possible implications for the inclusion of p-doped B:GaAs layers in NW heterostructures.

## 2. Method

### 2.1. Growth

Nanowires were grown via a self-catalyzed method directly on Si(111). The growth method was molecular beam epitaxy (MBE) at a substrate temperature of 630 °C. GaAs stems were grown for 18 minutes, under a V/III flux of ≈7, at an equivalent layer thickness growth rate of 0.1 μm $h^{-1}$, leading to NWs of length ≈1.35 μm. After this time, the B shutter was opened, and boron was supplied from a water-cooled high-temperature effusion cell loaded with powdered boron of 6N purity, at an operating

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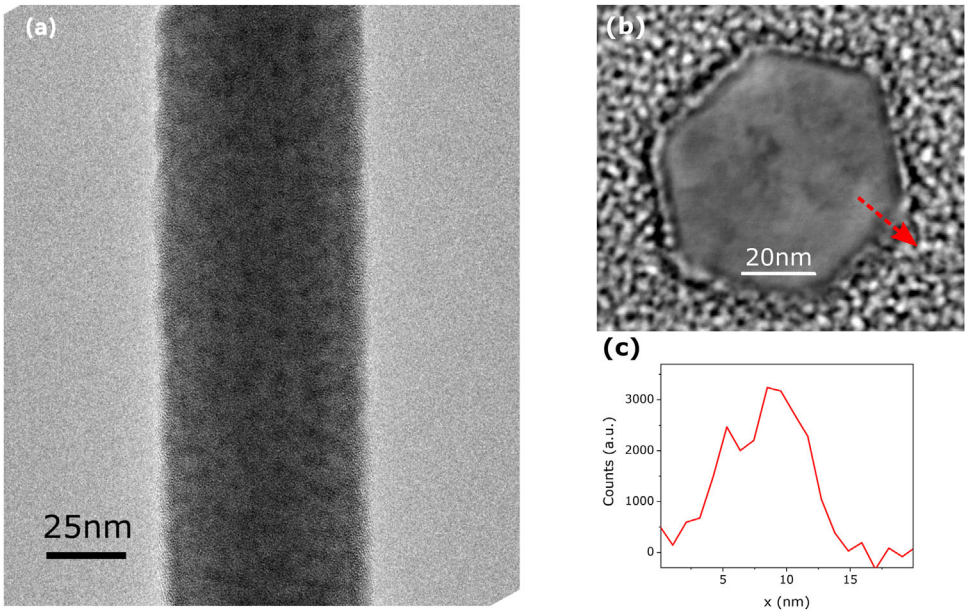


**Figure 1.** TEM analysis of NW surface: (a) HRTEM image of NW grown under boron flux; (b) cross-sectional TEM image of NW, indicating position of linescan used in EELS measurements; (c) intensity of background-subtracted EELS spectrum at energy loss of 194 eV with an integration width of 30 eV, taken along the linescan shown in (b).

temperature of 1725–1800 °C, leading to a nominal boron concentration of 0.22–0.36%, as measured from X-ray diffraction measurements on superlattice samples grown with the same cell temperatures.[10] The growth under boron flux varied between samples, either 30 or 42 min. After growth, the samples cooled down under residual $As_4$ flux.

The final NWs are of 1.59–2.06 μm length, depending on cell temperature. The unavoidable lateral overgrowth leads to slight tapering along the NWs, with the diameter at the tip (base) varying from 55 to 66 nm (62–98 nm), which again depends on both cell temperature and growth time. This growth method leads to a GaAs/B:GaAs core-shell structure along the nanowire.[14]

### 2.2. Processing and Measurement

Nanowires were prepared for high-resolution transmission electron microscopy (HRTEM) measurements to be taken both along the NW length and along a cross-section of the NW. Some nanowires were removed from the growth substrate via sonication in isopropanol and dispersed on 300-mesh copper grids with a carbon film. Additional pieces of the growth substrate were planarised using a Pt focused electron beam induced deposition (FEBID)-based technique[15] in order to look at the cross-sectional boron distribution.

For electrical measurements, contacts were defined on NWs using an e-beam lithography technique. NWs were dispersed on n-Si wafers with a resistivity of 1–5 $\Omega\,cm^{-1}$ covered with 50 nm dry thermal $SiO_2$. The substrates were first prepared via optical lithography for the deposition of pre-defined contact pads of Ti/Au. Back-gate contact pads were defined using optical lithography and a HF etch to remove the thermal oxide. Individual NWs were selected in scanning electron microscope (SEM) mode (in general, due to the low average length, the longest NWs were selected), and 2- or 4-point (pt) contact masks were defined, depending on NW length. A PMMA-based e-beam resist was spin-coated at 4000 rpm, with a thickness of 400 nm. After exposure and development, the contacts were metallized in a Balzers thermal evaporation system with either Cr/Au (5/100 nm) or Au/Zn/Au (5/10/100 nm). These metallization schemes were chosen due to the expectation of p-doping in the NWs. Further samples contacted with Ti/Au (5/100 nm) demonstrated Schottky contacts and low conductivity.

Electrical measurements were performed in ambient atmosphere at room temperature, on a Keithley 4200 semiconductor probe station. Au needles were used for contacting the contact pads and wires were measured in 2-, 4-pt and back-gated direct-current current–voltage (DC-IV) configurations, with a compliance of 1 μA and range of 1 pA. Sweep speeds were chosen to optimize for low-noise measurement.

## 3. Results and Discussion

The addition of boron during the growth of GaAs nanowires leads to the formation of boron-rich phases at the NW surface, leading to high surface roughening, as shown in **Figure 1**a. Electron energy-loss spectroscopy (EELS) confirms the presence of boron at the NW surface, with a peak appearing in the EELS spectrum centred on 194 eV (Figure 1b,c), indicating an inhomogeneous distribution of boron in the NW shell. The nominal concentration of boron is lower than should be detectable in the EELS measurements, thus we can conclude that there is surface segregation of boron leading to boron-rich phases which give the NW its rough surface and show up as dark spots in HRTEM images. This is an initial indication that the incorporation of B occurs predominantly on defect sites, rather than substitutionally on the lattice as expected.

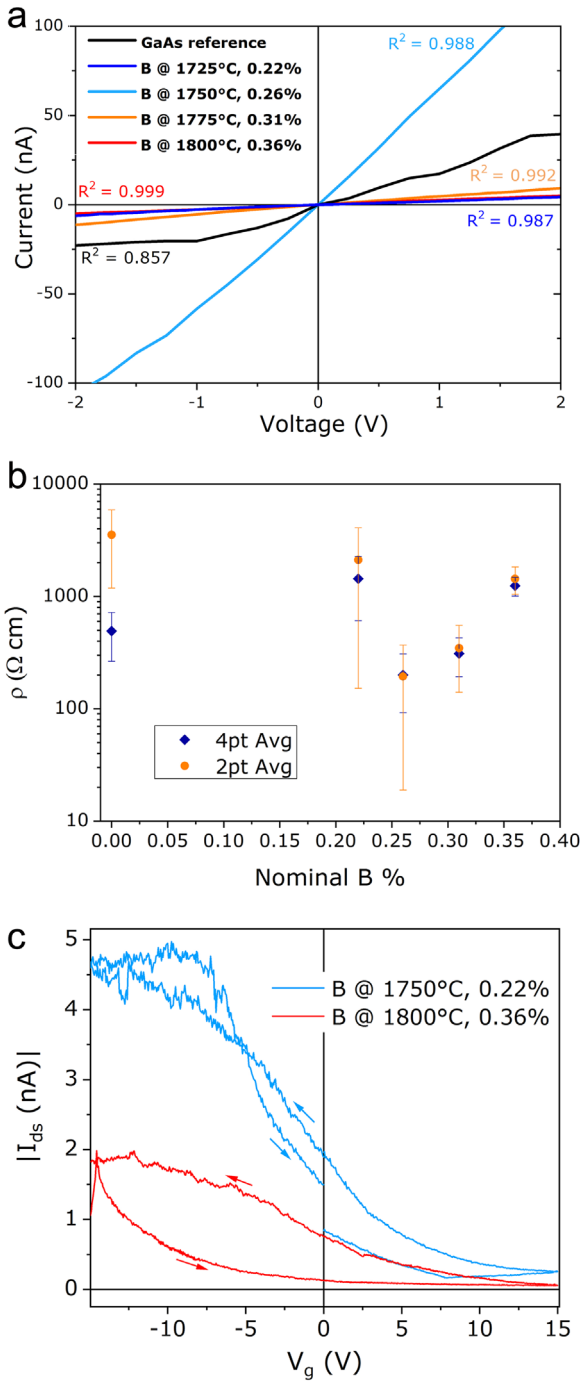


**Figure 2.** IV measurements on NWs: (a) representative 2-pt measurements on nanowires grown with and without boron, with $R^2$ values>0.95 indicating Ohmic behaviour; (b) comparison of 2- and 4-pt resistivities averaged over several NWs from each sample; (c) back-gated measurements taken on nanowires from two samples, with forward and reverse sweep indicated.

The IV curves for samples with different nominal boron concentrations as well as an undoped GaAs reference sample are shown in **Figure 2**b. Upon addition of boron to the GaAs nanowires, Ohmic contacts could be formed at all nominal boron

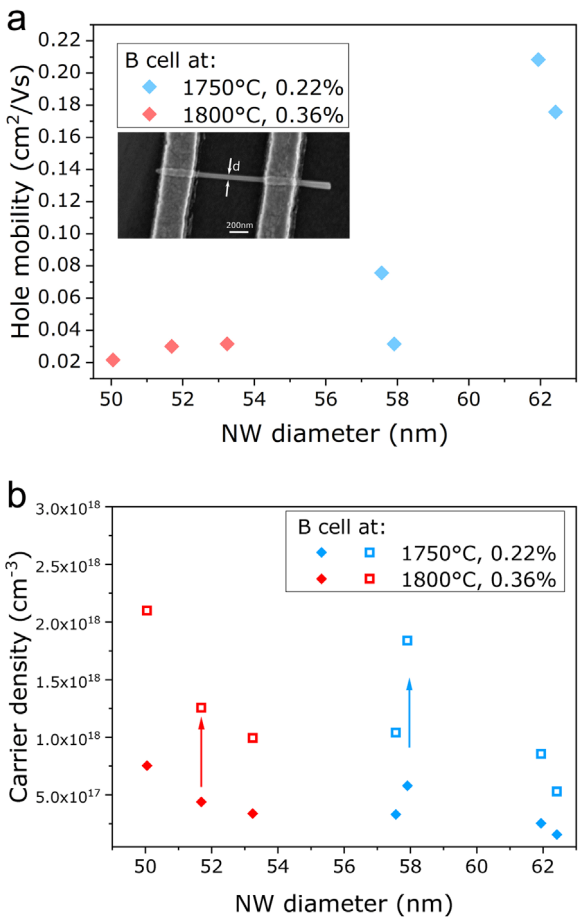


**Figure 3.** Calculated (a) hole mobilities (inset: SEM image indicating "diameter" of slightly tapered nanowire) and (b) carrier densities for a series of nanowires from two samples grown with the boron cell at different temperatures. In figure (b), diamonds represent carrier densities calculated assuming a homogeneous carrier distribution, and open squares represent densities assuming carriers are concentrated in a 5 nm shell near the surface.

concentrations. In contrast, similar contacts on undoped GaAs nanowires form Schottky contacts[16] due to the existence of a surface depletion layer in GaAs.[17] Enhanced conductivity in samples containing boron could be attributed both to doping of the nanowires, discussed further below, as well as an increased contact surface area due to the surface roughening visible in Figure 1a. Ohmic contacts were found for both metallizations, pointing to the p-type nature of the NWs.

Comparing the 2- and 4-pt resistivities of NWs grown under boron flux, we find that the contact resistivities of the NWs are very low compared to those found on undoped GaAs nanowires. This again indicates the high quality of contacts which can be formed upon the addition of small amounts of boron to GaAs nanowires. At low nominal boron concentrations, the NWs are still highly resistive, but the low contact resistance leads to low 2-pt resistivity. Slightly increasing the nominal boron content reduces the resistivity by an order of magnitude, but as the concentration is further increased the resistivity rises again, as discussed below. These data show that the addition of small

amounts of boron during NW growth can greatly improve electrical performance and contact quality.

Finally, back-gated measurements were performed on NWs in an field-effect transistor (FET) configuration. The backgate consists of 50 nm $SiO_2$ and contacts were formed using Au/Zn/Au. Some typical back-gated IV curves of NWs from samples with the highest and lowest B flux are shown in Figure 2c. These confirm the p-type behavior of the NWs, which could point to a large number of antisite defects acting as doubly-charged acceptors. A high hysteresis is visible, which we attributed to interfacial states between the NWs and the $SiO_2$ backgate, as well as the adsorption of oxygen and water molecules on the NW surface,[18,19] due to measurement in ambient atmosphere. The specific surface chemistry of the NWs due to the high boron concentration at the surface is still to be investigated.

From the back-gated IV curves, carrier mobilities and densities can be calculated following reference.[20] This leads to hole mobilities between 0.02–0.22 $cm^2 Vs^{-1}$ and carrier densities between $5 \times 10^{17} - 1 \times 10^{18}\,cm^{-3}$. Since the curves show high hysteresis, the subthreshold slope was extracted from the reverse sweep. The calculated hole mobilities and carrier densities are plotted in **Figure 3**. Carrier mobility falls in the NWs with a higher nominal boron concentration (Figure 3a), which we attribute to increased scattering due to increased roughness and a higher number of defects. The hole mobilities are in general low for the same reasons.

While the number of carriers slightly increases with nominal B content (Figure 3b), indicating higher p-doping levels as the B cell temperature is increased, the reduced carrier mobility and increased resistivity of NWs grown at the highest B flux (Figure 2b) suggests that carrier scattering increases and may point to a lower material quality as the nominal B content increases. Thus while the addition of boron can be used to tune the NW conductivity, the growth parameters should be further optimized in order to improve control over defect incorporation and increase the potential tuning range.

The extracted carrier densities (Figure 3b, diamonds) also appear low for forming Ohmic contacts in NWs.[17] Taking these values and using them in calculations for the expected depletion width,[21] using real nanowire diameters, we find that the NWs should be almost fully depleted. This can be explained by the fact that we use the full nanowire radius for the carrier density calculations, thus a homogeneous distribution of carriers is assumed. If we instead assume that the carriers are concentrated in the "shell" region, near the NW edge, we can recalculate the carrier densities. An example is plotted in Figure 3 (open squares) assuming carriers are concentrated in a radial NW shell of ≈5 nm, and in this case the carrier densities are higher, although still below those found in Hall measurements on planar samples,[10] which are on the order of $10^{19}\,cm^{-3}$.

## 4. Conclusion

The addition of boron during the MBE growth of GaAs nanowires was investigated electrically. Segregation of boron to the surface was confirmed via HRTEM and EELS and leads to a high surface roughness. Through tuning of the growth parameters, it is expected that boron can be incorporated substitutionally in $B_xGa_{1-x}As$ layers for strain engineering in nanowire heterostructures, or on antisite defects for doping of GaAs NWs.

2-pt measurements indicated good formation of contacts to nanowires grown under boron flux, and comparison with 4-pt measurements showed that the contact resistance of these wires was low. Back-gated IV measurements allowed for the calculation of carrier densitites, which reached $2 \times 10^{18}\,cm^{-3}$, assuming a high concentration of carriers near the surface. These results demonstrate that the incorporation of boron on antisite defects can be used for the formation of Ohmic contacts with low contact resistances to B:GaAs nanowires.

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## Conflict of Interest

The authors declare no conflict of interest.

## Keywords

B:GaAs, boron doping, molecular beam epitaxy, nanowires

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