Performance of a Two-Stage Actively Damped LC Filter for GaN/SiC Motor Inverters

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***Abstract*—In this paper, the filter performance of a wide-bandgap (WBG) three phase motor inverter with integrated sinusoidal output voltage LC filter is analyzed. To ensure a well damped system behaviour at low losses, an active damping scheme based on filter capacitor feedback is used. Unfortunately, the nonlinear DC-Bias dependent capacitance of the used ceramic capacitors (X7R is used to minimize filter volume) significantly affects the active damping. A symmetrical filter structure sufficiently reduces the capacitors voltage dependency. However, the paper shows that the symmetrical structure also causes negative effects in respective to the filters noise suppression performance. Modifications in the filter topology are reported and analyzed for reducing the impaired noise suppression. The proposed filter scheme finally results in a well damped system behaviour fulfilling established EMC standards according output noise demonstrated by experimental results of a 2 kW / 400 V laboratory prototype.**

I. Introduction

During the past few years, wide bandgap switching devices like GaN- and SiC MOSFETs have considerably emerged, also in inverter applications based on $600\,\mathrm{V}$ GaN devices. The low semiconductor capacitances of GaN as well as advances in packaging technologies facilitate very high switching speed resulting in substantially lower switching losses in comparison to silicon (Si) based IGBTs. Due to the low switching- and also low on-state losses of GaN MOSFETs, motor inverters with high efficiency rates rather at high switching frequencies are feasible [1]. However, the high switching speed of these transistors with rise times down to $10\,\mathrm{ns}$ at $400\,\mathrm{V}$ DC-link voltage also create some crucial issues for motor applications caused by high du/dt rates of the inverter output voltage addressing the inverter-to-motor wiring system and possible machine lifetime impacts due to du/dt and/or transient overvoltages.

On the other hand, high switching frequencies also opens the possibility to implement a filter system directly into the GaN inverter which suppresses all switching frequency harmonics such that motor and cabling are fed by sinusoidal-like voltages, avoiding the problems addressed previously. With this, furthermore it seems to be possible to avoid shielded motor cables, resulting in an appealing cost and application benefit. For the aimed filtering, a two-stage LC topology is used to achieve sufficient switching noise attenuation but also to guarantee a rather high current control bandwidth [2] as being necessary, e.g., for servo drives.

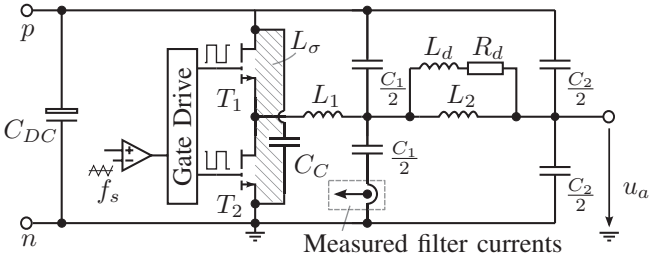

Fig. 1. Schematic concept of the proposed motor inverter with GaN-power stage, actively damped symmetrical two-stage filter for a 3-phase motor as load.

In [3], a filter is designed such that at the output of the inverter unit a noise level according to EN55011 class-A is aspired to comply with common industrial EMI standards. It implicates that in the frequency domain of $150\,\mathrm{kHz}$ to $500\,\mathrm{kHz}$ the output voltage noise has to be lower than $79\,\mathrm{dB\,\mu V}$. A schematic concept of the inverter with GaN-power stage is depicted in Fig. 1. However, the resulting resonances of the passive LC sine wave filter have to be damped. To obtain high inverter system efficiencies, instead of dissipative damping an active damping scheme by feedback of the capacitor filter currents is implemented [3] for the first filter-stage. As described in [4], the active damping emulates a kind of ohmic (but not-dissipative) damping resistor leading to a well damped system if the feedback coefficient properly is tuned to the filters L and C values. However, the voltage dependent capacitance of the filters X7R ceramic capacitors (which are preferred to achieve a high power density as well as a good frequency response in the high frequency (hf) region) will show a negative impact on the active damping. Hence, a filter topology being symmetrical with respect to the DC-link is proposed which substantially reduces the effect of capacitors voltage dependency guaranteeing a stable behaviour of the actively damped inverter.

The proposed symmetrical filter structure in the basic topology however unfortunately also degrades the switching noise suppression as will be addressed in the next section. Therefore,

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the filter is modified to a quasi-symmetrical structure to comply with the aspired EMC standard illustrated in Section III.

II. Inverter Filter Performance

A filter design for an inverter with a rather high control bandwidth is discussed in [3], which theoretically fulfil the chosen EMC standard without consideration of parasitic component characteristics. The obtained filter parameters are listed in Table I. In reality, the amount of emissions in the MHz domain strongly depends on the geometry of the commutation loops as well as on the parasitic properties of the filter components, which degrade the filter performance especially in the high frequency region.

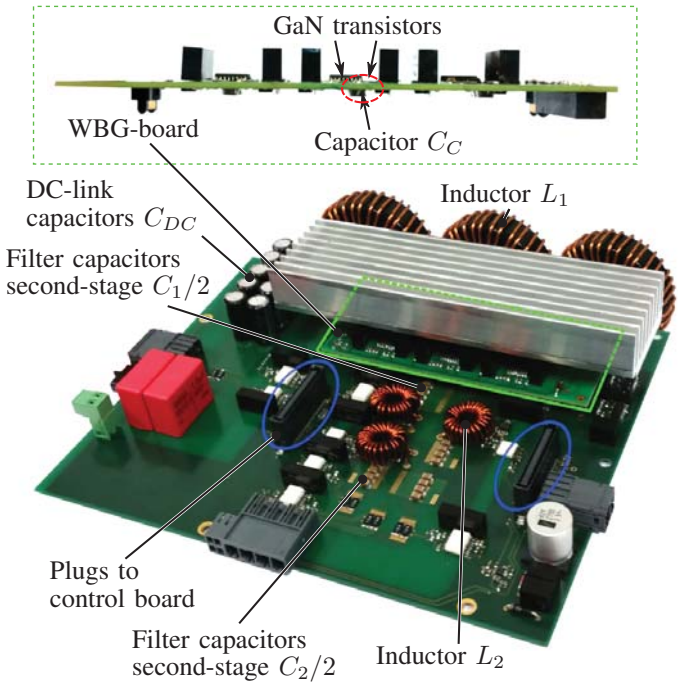

Fig. 2. Laboratory prototype: WBG- and power-board with implemented symmetrical two-stage filter. Dimensions power-board: 200 mm x 250 mm.

A. Experimental Setup

A 2 kW/400 V 3-phase WBG inverter laboratory prototype operating at a switching frequency of 100 kHz is used to test the filter performance of the implemented symmetrical two-stage filter (Fig. 2). The laboratory prototype mainly consists of three different PCB boards, a wide bandgap transistor carrier- (WBG), a power- and a control-board. GaN-HEMTs GS66506T are used as active switches for the three half-bridges on the WBG-board. DC-link ceramic capacitors C_C are placed directly underneath the GaN transistors for minimizing the parasitic inductance L_σ of the commutation loop in order to reduce transient switching overvoltages (Fig. 2, top). The implemented two-stage filter is placed on the power-board. For the filter inductors of the first and second stage, toroidal powder core chokes are assembled showing rather low core losses as well as a relatively high saturation current limit,

TABLE I
Parameter settings for laboratory prototype measurement.

Part	Parameter	value	unit
Inverter	U_{DC}	400	V
	C_{DC}	120	µF
	f_s	100	kHz
Sine filter	L_1	200	µH
	C_1	2.5	µF
	L_2	25	µH
	C_2	2.5	µF
	L_d	25	µH
	R_d	2.5	Ω

resulting in a peak over-current capability of about 1:3 (which is necessary for motor applications). The coils are formed as single layer windings to minimize the proximity effect using standard copper wire as well as to reduce the parasitic winding capacitances in order to achieve adequate frequency response characteristics of the inductors up to the MHz domain. Above 10 MHz, however, coupling effects between the individual inductors and the capacitors can degrade the desired filter performance. These effects can be reduced by a proper placement of the components on the power-board or by magnetic shielding [5].

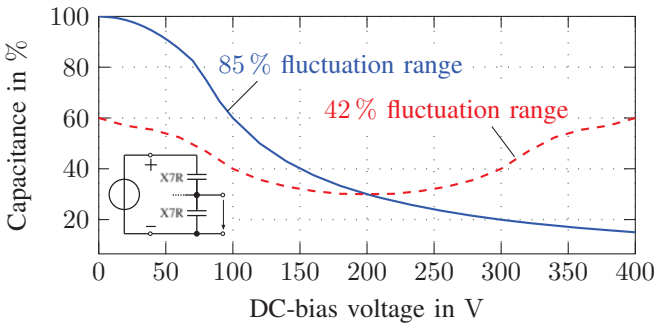

Fig. 3. Capacitance dependence of a MLCC ceramic capacitor Arcshield X7R, 330 nF/500 V on the DC-bias voltage (blue). Capacitance variation of the proposed symmetrical filter structure based on two X7R filter capacitors connected to +/- DC-link (red dashed).

In addition to the inductors, the frequency response of the filter system is mainly determined by the used capacitors. In comparison to film capacitors, ceramic capacitors like e.g. X7R are rather compact resulting in high system power density and better frequency characteristics due to lower parasitic inductances being essential to meet the required EMC standards at high frequencies. In contrast, film capacitors are characterized by precise and constant capacitance ratings being not dependent on the applied DC voltage level. Hence, they are used in common inverter sine filter applications [6]. Ceramic capacitors in recent years demonstrate remarkable technology advances resulting in exciting specific capacity densities, especially also at higher voltage ratings up to 500 V...1000 V.

These components however, show very pronounced nonlinear behaviour in terms of DC-bias voltage (cf., Fig. 3). Hence, the filter cut-off frequency will rise at high inverter output voltage and thus impair noise rejection. Furthermore, as mentioned above, stability problems of the inverter may occur due to the implemented active damping which is affected by the variation of the capacitance. To avoid this heavily nonlinear characteristic, a simple symmetrical filter structure is proposed consisting of two capacitors connected from the inductor output to the positive as well as to the negative DC-link rail. This actually is an AC parallel connection via the DC- link capacitor but a DC series connection such at least one capacitor will show high capacitance at high inverter modulation rate. With this the voltage-dependent reduction of the filters effective capacitance largely is improved (cf., Fig. 3) maintaining noise suppression and stability margin of the active damping. For the implemented motor inverter, MLCC ceramic capacitors (Archshield X7R, 500V) are used for first and second filter-stage to handle the occurring switching frequency ripple. The DC-link capacitance is formed by EEUED2W150 aluminium electrolytic capacitors $15\,\mu\text{F}/450\,\text{V}$, which can absorb the appearing current ripple at high frequencies.

The switching frequency noise characteristic of the inverter system is tested by measuring the spectrum of the filter output voltage. For this, the motor inverter operates as a buck converter under no load, at a DC-link voltage of $U = 400\,\text{V}$, a switching frequency of $f_s = 100\,\text{kHz}$ and a duty cycle of $50\,\%$ (worst case scenario). Due to the short interlock delay of $150\,\text{ns}$ compared to the set switching frequency, a rectangular voltage is assumed to be applied at the filter input (influence of interlock delay time on EMI-performance is illustrated in [7]). As a result, odd-numbered switching frequency harmonics are expected at the filter output. For the measurement, a Rigol DSA0815TG spectrum analyzer is used, being able to measure in a frequency range of $9\,\text{kHz}$ to $1.5\,\text{GHz}$.

In Fig. 4, the measured output voltage spectrum is depicted between $100\,\text{kHz}$ and $40\,\text{MHz}$ (blue trace). In addition to the expected odd-numbered components ($100\,\text{kHz}$, $300\,\text{kHz}$,...) pronounced even-numbered harmonics ($200\,\text{kHz}$, $400\,\text{kHz}$,...) are observed which violate the intended EMC standard. For clarification of this effect, the two-stage filter is reduced to a simple single-stage symmetrical filter by removing L_2, C_2, R_d, L_d. The obtained frequency spectrum however still shows even-numbered harmonics in about equal magnitude as for the two-stage filter (cf., Fig. 4).

B. Noise Loop Analysis

In order to find the physical source of this phenomenon an adequate equivalent circuit has to be evolved. In a first step, the circuit of Fig. 1 is extended by parasitic filter elements and wiring inductances L_w. It has to be noted, that this model depicted in Fig. 5 does not consider inductive and capacitive coupling effects, as they typically affect a frequency range beyond $10\,\text{MHz}$ and thus they are not held responsible for the occurrence of the reported $200\,\text{kHz}$, $400\,\text{kHz}$,... harmonics.

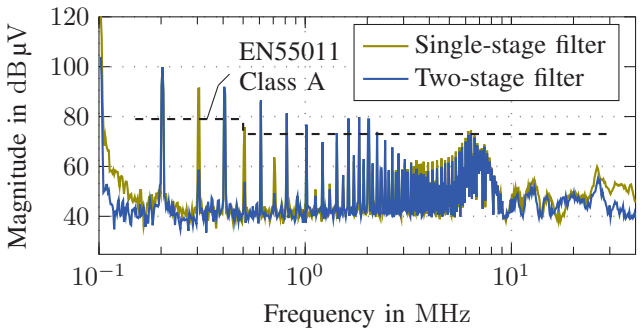

Fig. 4. Comparison of measured frequency spectrum for the symmetrical two-stage (blue) and single-stage (green) filter. Spectrum analyzer parameters: Gauss-Filter and Positive-Peak-Detection, 9 kHz resolution bandwidth (RBW).

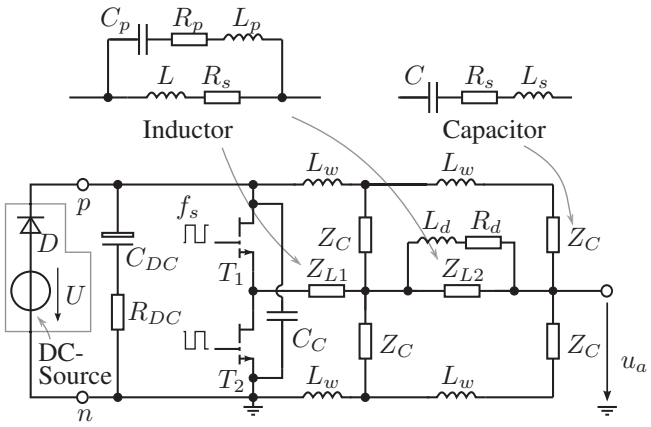

Fig. 5. Single-phase equivalent circuit of the proposed motor inverter including parasitic filter components.

To determine the parasitic filter elements, impedance measurements of the filter components are used, shown in Fig. 6, wherein the obtained resonance frequencies can be represented by $f_r = 1/\left(2\pi\sqrt{L_x C_x}\right)$ with $x \in \{s, p\}$. The first (i.e. parallel) resonance frequency of the filter inductors defines their parasitic winding capacitance C_p, the second (serial) resonance is modelled by an inductance L_p in series to C_p. In the case of capacitors, the package size has a significant influence on the frequency characteristics. Here, a small package and

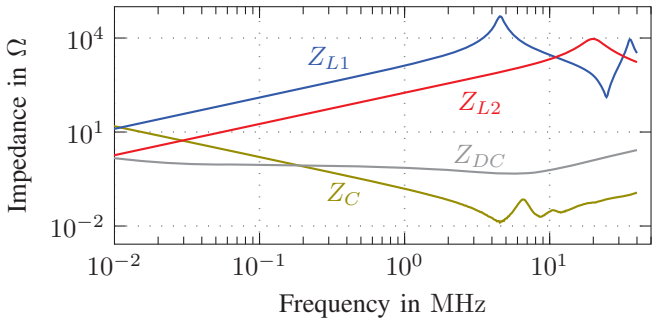

Fig. 6. Frequency dependent impedance sweep of the passive inverter components, measured with Bode100 analyzer.

short terminals result in a low stray inductance L_s and high resonance frequency [8]. The identified parasitic component parameters are listed in Table II.

TABLE II
PARAMETER SETTINGS FOR INVERTER MODEL WITH PARASITIC COMPONENTS.

Part	Def	value	unit	Part	Def	value	unit
Z_{L1}	L	200	µH	Z_{L2}	L	25	µH
	R_s	0.11	Ω		R_s	0.05	Ω
	C_p	6.2	pF		C_p	2.4	pF
	L_p	6.7	µH		L_p	0	µH
	R_p	150	Ω		R_p	500	Ω
Z_C	C	1.25	µF	Z_{DC}	C_{DC}	120	µF
	R_s	11	mΩ		R_{DC}	0.2	Ω
	L_s	56	nH	Wire	L_w	60	nH

A simulation of the model including parasitic filter elements in GeckoCircuits also shows the occurrence of even-numbered switching frequency harmonics. Furthermore, the measured spectral components in the range between 100 kHz to 15 MHz can be adequately reproduced by the proposed model. Between 100 kHz to 1 MHz the filter components however virtually show ideal properties (cf., Fig. 6), hence, it is not the case that the parasitic effects cause or have influence on the amplitudes of the even switching frequency harmonics demonstrated in Fig. 4 . Thus, most of the parasitic filter elements can be neglected for this frequency range except of the DC-link capacitors, which are dominated by their ohmic loss part R_{DC} for frequencies higher than 20 kHz (cf. Z_{DC} in Fig. 6).

C. Symmetrical Filter Structure

For clarifying the appearing additional noise (even) harmonics, a symmetrical single-stage filter is analyzed briefly first. By consideration of the impedance measurements, a simplified equivalent circuit valid for the range between 100 kHz to 1 MHz is specified (cf., Fig. 7a). It is assumed, that the inverter operates as a buck converter under no-load condition at 100 kHz, where the filter input voltage depends on the duty cycle of the half-bridge. In case of ideal switches instead of the GaN MOSFETs as well as a chosen duty cycle of 50 %, a symmetrical triangular-shaped inductor current results, flowing into the two filter capacitors. Under the condition that T_1 is on, circuit Fig. 7b is valid. This noise model now leads to the equations

$$i_{C_C} = C_C \frac{\mathrm{d}u_{C_C}}{\mathrm{d}t} = C_C R_{DC} \frac{\mathrm{d}i_{DC}}{\mathrm{d}t}, \tag{1a}$$

$$i_{C12} = i_{C_C} + i_{DC}, \tag{1b}$$

$$i_{C11} = C_{11} \frac{\mathrm{d}u_{C11}}{\mathrm{d}t} = C_{11} \left(\frac{\mathrm{d}u_{C12}}{\mathrm{d}t} + R_{DC} \frac{\mathrm{d}i_{DC}}{\mathrm{d}t} \right), \tag{1c}$$

and

$$i_{L1} = i_{C12} + i_{C11}, \tag{1d}$$

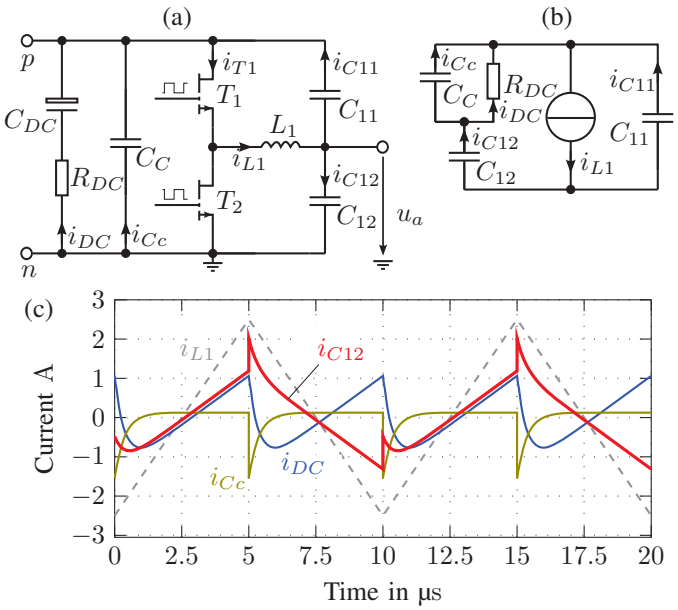

Fig. 7. (a) Half-bridge with symmetrical single-stage filter and (b) corresponding noise model for the range 100 kHz to 1 MHz. (c) Analytically calculated noise model currents.

from which the differential equation

$$\frac{\mathrm{d}i_{DC}}{\mathrm{d}t} = K_1 i_{DC}(t) - K_1 \frac{C_{12}}{C_{11}+C_{12}} i_{L1}(t), \tag{2}$$

with

$$K1 = -\frac{C_{11}+C_{12}}{R_{DC}\left(C_{11}C_{12}+C_{11}C_C+C_C C_{12}\right)}.$$

can be derived, as a function of i_{L1}. Here, it is assumed that $C_{11} = C_{12} = C_1/2$ is valid. For a full switching period $T_s = 1/f_s$, the inductor current i_{L1} can be specified as

$$i_L(t) = -\hat{I}_T + \frac{2\hat{I}_T}{T_s/2} t, \quad 0 \le t < T_s/2, \tag{3a}$$

$$i_L(t) = \hat{I}_T - \frac{2\hat{I}_T}{T_s/2}(t - T_s/2), \quad T_s/2 \le t < T_s, \tag{3b}$$

with $\hat{I}_T = 1/(2L_1)U(1-\delta)\delta T_s$. By analytically solving of (2), the DC-link current can be written as

$$i_{DC}(t) = A + Bt + De^{K_1 t}, \tag{4}$$

with

$$A = -\frac{C_{12}}{C_{11}+C_{12}} \frac{\hat{I}_T K_1 - 4\hat{I}_T/T_s}{K_1}, \tag{5a}$$

$$B = \frac{C_{12}}{C_{11}+C_{12}} 4\hat{I}_T/T_s, \tag{5b}$$

$$D = I_{DC,0} + \hat{I}_T \frac{C_{12}}{C_{11}+C_{12}} \left(1 - \frac{4}{T_s K_1}\right). \tag{5c}$$

Due to the used noise model the DC-link current $i_{DC}(t)$

is continuous. Hence, the initial condition $I_{DC,0}$ can be well approximated by $I_{DC,0} = i_{DC}(t = T_s/2)$, since the influence of the exponential term in (4) is already negligible at this time instant. For the time interval $T_s/2 \leq t < T_s$ the transistor T_2 is on (T_1 is off). Therefore, the structure of the differential equation for i_{DC} is equal to (2), only the positions of C_{11} and C_{12} need to be changed. Thus, $i_{DC}(t)$ can be represented over a full switching period, as illustrated in Fig. 7c. In contrast to a single-ended filter, where the DC-link current always corresponds to a switching frequency periodic signal, i_{DC} in the symmetrical structure has now a period of $1/(2f_s)$. The filter currents of the output capacitors can be obtained via (1b) and (1d) and hence, the spectral frequency components of the output voltage u_a can be calculated [9], shown in Fig. 8. Due to the 200 kHz DC-link current, u_a contains significant amounts of corresponding (even-numbered) harmonics.

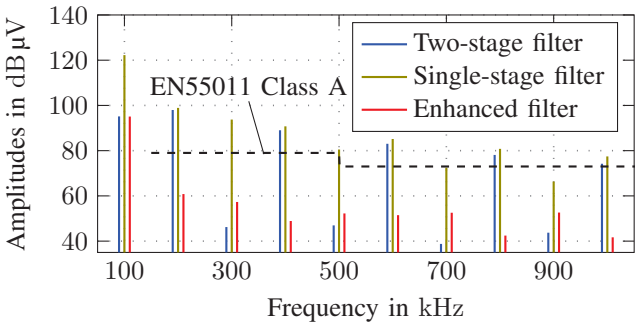

Fig. 8. Simulated output voltage frequency components for the considered filter topologies (single-stage, two-stage symmetrical, two-stage enhanced).

For the two-stage symmetrical filter the noise model has to be extended by the filter components C_{21}, C_{22} and L_2, as illustrated in Fig. 9a. Due to the symmetrical filter structure, the capacitances are defined to $C_{21} = C_{22} = C_2/2$. Again, the filter inductor current i_{L1} represents the input quantity. A simulation of this noise model in GeckoCircuits provides the resulting DC-link as well as filter currents (cf.,Fig. 9b). As for the single-stage filter, i_{DC} has a period corresponding to twice the switching frequency of the bridge leg and the filter capacitor i_{C22} shows also harmonics at twice the switching frequency. The resulting output voltage spectral components are listed in Fig. 8. It is obvious, that the even-numbered switching frequency harmonics do not exhibit a significant additional attenuation by the second filter-stage and violate the specified limits of the EMC standard EN55011.

III. Improvement of Filter Performance

As mentioned above, the load current ripple for the symmetrical filter structure leads to DC-link capacitor currents showing also harmonics of twice the switching frequency resulting in corresponding DC-link voltage harmonics because of the non-zero impedance Z_{DC} of the DC-link. These voltage harmonics are directly transferred to the filter output voltage with only minor attenuation via capacitors C_2. Actually the

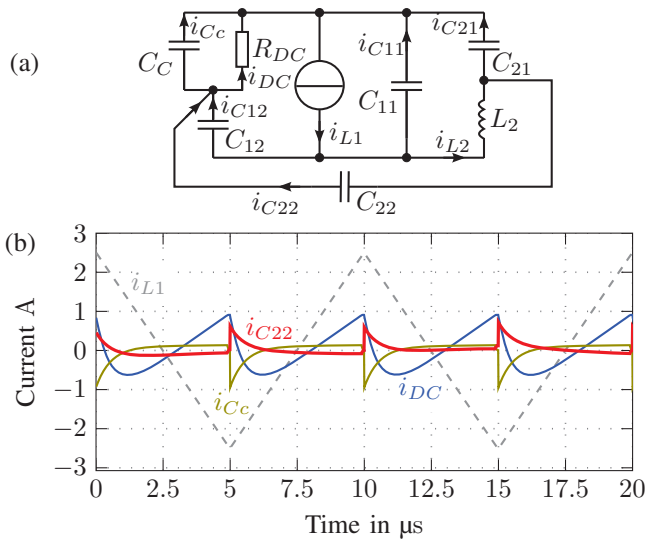

Fig. 9. (a) Noise model for the symmetrical two-stage filter in the range of 100 kHz to 1 MHz. (b) Simulated currents of the noise model.

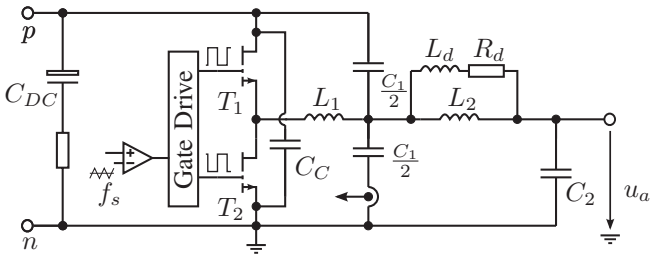

Fig. 10. Single-phase circuit diagram of the inverter system with enhanced output filter.

two capacitors $C_2/2$ form a 1:1 (6 dB) capacitive voltage which bypasses the filter inductor.

The filter performance can be improved by lowering the switching frequency components of u_{DC} as a result of reducing Z_{DC} (i.e. mainly be reduction of the equivalent series resistor R_{DC} in case electrolytic capacitors are used). In practice, this requires a parallel arrangement of several devices, or a considerable number of additional DC-link ceramic devices in parallel to the electrolytic capacitor. However, since typically less than 10 mV switching noise must be achieved in order to comply with the EMC standard, this procedure is not effective as a stand-alone measure. It has to be noted, that the mentioned additional output voltage noise would not appear if the filter stages are equipped by single capacitors from output to GND. However, the symmetrical structure of first filter-stage is necessary for an adequate compensation of the voltage dependency of the used X7R ceramic capacitors (which show the advantage of small volume and high ripple current capability). Although, the second filter-stage uses also the X7R capacitors, its symmetrical structure advantageously is replaced by a single-ended variant (Fig. 10), which is possible due to the passive damping of the second resonance frequency by $R_d L_d$. Thus, the described switching noise

(including even-numbered harmonics) appearing at the output of the first filter-stage receives a sufficient attenuation by the second stage which does not suffer from the reported bypass effect and so the EN55011 class A standard can be met.

A. Experimental Results

The output filter of the existing 2 kW/400 V DC laboratory prototype operating at a switching frequency of 100 kHz has been modified to a single-ended second filter-stage, as illustrated in Fig. 10. Measurement results of the laboratory prototype, operating as a buck converter at no-load condition, are depicted in Fig. 11 including first-stage filter inductor current i_{L1} and output voltage AC-part for the symmetrical (green) and the enhanced (black) filter system. Already these time diagrams indicate a much better output noise behaviour of the proposed enhanced filter, clearly visible especially at switching instants of the half-bridge.

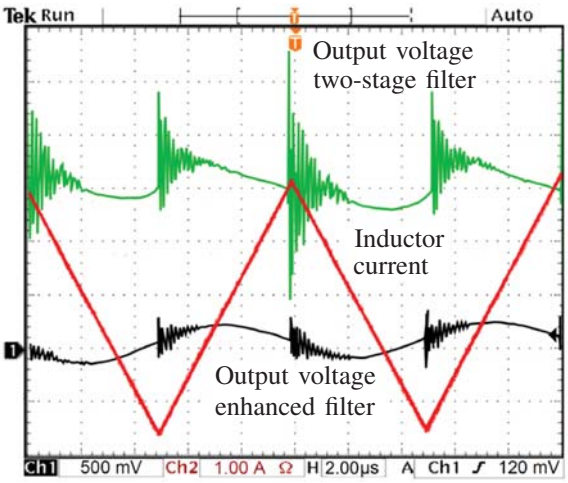

Fig. 11. Inductor current i_{L1} (red) and output voltage AC noise ripple (green) for the two-stage symmetric filter as well as for the proposed enhanced filter (black). Inverter parameters: buck-converter no-load operation at $U = 400\,\mathrm{V}$, $\delta = 50\,\%$.

This improvement is even more demonstrated by the spectral measurements of Fig. 12. Especial the even-numbered harmonics (200 kHz, 400 kHz,) substantially are improved by the enhanced second filter-stage (Fig. 12a). A measurement using the spectral analyzer in EMI-pre-compliant filter and detector mode confirms that the inverter output voltage conforms to EN55011 Class A level at no-load condition (cf., Fig. 12b). In addition, also the variation of the output voltage spectrum in case of an ohmic load at the inverters output is illustrated. The occurring DC current increases the switching speeds of the used WBG transistors and leads to a deterioration of the frequency behaviour for frequencies higher than 5 kHz. However, the chosen standard can still be met.

IV. Conclusion

In this work, the design of an output voltage sine filter for a 3-phase WBG motor inverter, operating at 400 V DC-link voltage at a PWM frequency of 100 kHz is analyzed. For

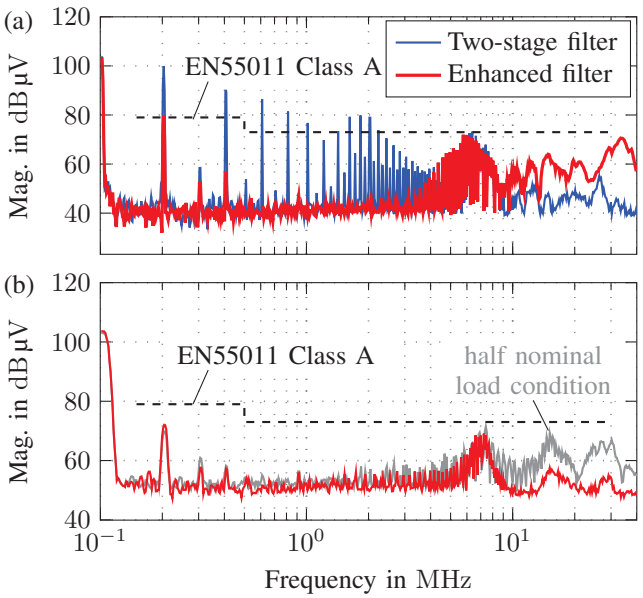

Fig. 12. Measured frequency spectrum of output voltages. Spectrum analyzer parameters: (a) Gauss-filter and positive-peak-detection, (b) EMI-pre-compliance filter and positive-peak-detection, 9 kHz resolution bandwidth(RBW), for no load (red) and half nominal load (gray) conditions.

achieving higher system efficiencies, active filter damping by capacitor current feedback is implemented. For minimizing the physical size ceramic X7R components are used as filter capacitors, which, however, are characterized by a substantial capacity dependency on the DC-bias voltage influencing the filter response and the active damping. To mitigate this effect a symmetrical filter topology (i.e., split-up into two capacitors connected to negative and positive DC-link rail) is proposed. This, however bypasses the filter inductor to some extent and degrades the switching frequency output voltage noise due to the non-zero hf impedance of the DC-link. In addition, also not expected output voltage harmonics originating from the inductor current ripple may appear. Simulations show, that this drawback sufficiently can be handled by a single-ended implementation of the second filter-stage. The proposed modified filter structure is verified by an existing laboratory GaN inverter prototype, and demonstrates that the system complies with the aspired EMC standard EN55011 class A.

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