VELS- VHDL E-Learning System for Automatic Generation and Evaluation of Per-Student Customized Tasks for Hardware Modeling Courses

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VHDL (Very High Speed Integrated Circuit Hardware Description Language) is a powerful hardware description language to design algorithms and functionalities to be automatically converted to digital circuits. It is an important instrument for electrical engineering students. Unfortunately, decreasing teacher-to-student ratios limit the possibilities to offer personalized guidance based on students' needs. The goal of the VHDL E-Learning System (VELS) is to give students the possibilities to learn at their own pace and learn from their own mistakes while considering their previous knowledge.

Once started, VELS fully automatically generates individualized tasks, handles submissions, and gives feedback in order for students to iteratively solve a given problem. The different versions of the same task are parameterized, so no students get the exact same task. For students, VELS provides an easy to use email interface. For teachers VELS offers flexibility through: intuitively assisting in defining new tasks, an interface to add support for different simulation backends, and different course scheduling modes. So far, 20 different task families have been implemented and VELS has helped over 1000 students in three years and in six courses to grasp concepts for building complex hardware designs. VELS is published under the open source license GPLv2.