FWF-Proposal DMAC: Digital Modeling of Asynchronous Integrated Circuits for Fast Dynamic Timing Analysis and Formal Verification

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Abstract

The project proposal *Digital Modeling of Asynchronous Integrated Circuits for Fast Dynamic Timing Analysis and Formal Verification* (DMAC) is devoted to the development of a purely digital model for asynchronous circuits, which enables accurate and fast dynamic timing analysis and is a mandatory prerequisite for any attempt on practical formal verification of such designs. The envisioned model shall be accurate and realistic (= faithful), in the sense that the behavior of circuits described in the model is exactly, i.e., within the modeling accuracy, the same as the behavior of the corresponding real circuit. In contrast to analog models, which are known to be faithful but suffer from excessive simulation times, we target continuous-time discrete-value models here, which essentially boil down to elaborate delay models for gates and/or interconnecting channels.

This proposal emerged from some discoveries obtained in the context of two recent FWF projects, where we happened to realize the importance of the scientific questions to be addressed in DMAC from two very different angles: As a basis for correctness proofs of fault-tolerant digital circuits and as a mandatory prerequisite for practical formal verification of reasonably large asynchronous circuit designs. In our attempts to get a first grip on these scientific questions, we discovered a new channel model that differs from almost all existing ones in that the input-to-output delay depends on the history in the signal traces. Most importantly, we identified delay functions that are mathematical involutions as being key for faithfulness, in the sense that we managed to rigorously prove that our involution channels are the only candidates for a faithful digital circuit model known so far.

DMAC is devoted to fully explore this avenue scientifically. The most challenging open questions that shall be answered in this project are how to enlarge the class of circuits where the involution model and variants thereof are faithful, how to compose gates with different electrical properties, in particular, different threshold voltage levels, how to accurately model subtle delay variation originating in the Charlie effect in multi-input gates, how to parametrize and characterize the model for a given technology and given operating conditions, and how to possibly further improve the modeling coverage and accuracy. In addition, we will also incorporate our models into existing timing analysis and verification tools. Besides demonstrating the practical feasibility of our approach, this is a mandatory step for experimentally evaluating the accuracy of our models.

Keywords: *Digital integrated circuits, continuous-time delay modeling, dynamic timing analysis, model composition, correctness proofs, formal verification.*

1 Scientific Aspects

1.1 Introduction and Project Overview

The "digital revolution", which nowadays transforms our society in an unprecedented way, essentially rests on two fundamental pillars: *Discretization* of the (usually continuous) world, which dramatically reduces the complexity of problem solving, and *executable models*, which allow a *machine* to compute model predictions. Not surprisingly, this revolution has also transformed its own basis, namely, the hardware of computer systems: Despite being built from continuous-value continuous-time analog electronics at the end, provided by nanometer-range VLSI technology, it is nowadays designed solely by means of various digital abstractions, which allow to build Billion-transistor chips within reasonably short design and test cycles.

Among the key technologies of modern digital circuit design are fast timing analysis techniques. State-of-the-art *static* timing analysis tools like Synopsis Prime Time are able to very accurately predict the timing behavior of a given synchronous[1] circuit design, and to identify setup/hold-violations and other timing-related problems. Since they do not involve any signal trace-related considerations, however, *dynamic* timing analysis techniques must be resorted to for those parts of a circuit where e.g. the presence of glitch trains may severely affect correctness and power consumption [55, 24]. Whereas dynamic timing analysis is only performed for critical parts of a circuit nowadays, it is safe to predict that the demand for dynamic timing analysis will grow in the future. The need for trace-related timing considerations is even more important for any attempt to formally verify the correctness of a given circuit design. After all, its potential to uncover race conditions, hazardous glitches and other corner-case effects relevant for timing-closure analysis is one of the main drivers for pushing verification of digital circuits. Suitable foundations for a rigorous and not overly conservative timing analysis of complex circuits are obviously a mandatory prerequisite here.

And indeed, the need for scientific research on the topics dealt with in the proposed project emerged from two different research projects conducted recently in our research group, namely, the stand-alone FWF project SIC[2] and the FWF National Research Network RiSE/SHiNE[3]: SIC, devoted to fault-tolerant asynchronous circuits, revealed the importance of accurate dynamic timing analysis for developing correctness proofs, whereas the participation in RiSE/SHiNE allowed us to learn about the potential and limitations of existing formal verification approaches for circuits that are not completely synchronous. The first thing to note in this context is that statements about the correctness of a circuit *in a model*, which is what dynamic timing analysis and formal verification can provide, are meaningful only if they also imply correctness of the corresponding *real* circuit implementation. We hence call a model *realistic*, if a given problem can be solved in the model if and only if it can be solved by a real circuit, and *faithful* if it is both realistic and provides accurate timing predictions.

The "golden standard" for dynamic timing analysis nowadays are fully-fledged analog simulations,

[1] A synchronous circuit consists of combinational logic blocks separated by flip-flops, which are driven by a common clock signal. Its computation can be accurately described by a binary-value, discrete-time model, which assumes that the discrete state of the circuit at time t is computed by processing the state previously computed at time $t-1$. The clock frequency must be chosen appropriately to avoid setup/hold violations, e.g., due to data signals coming from slow logic blocks that do not stabilize before the next clock transition.

[2] FWF project SIC (Self-stabilizing Byzantine Fault-Tolerant Distributed Algorithms for Integrated Circuits, P26436).

[3] FWF NfN RiSE/SHiNE (Rigorous Systems Engineering, S11405), a large national research network project, see https://arise.or.at/nfn/shine-organization-and-subprojects/ for an overview.

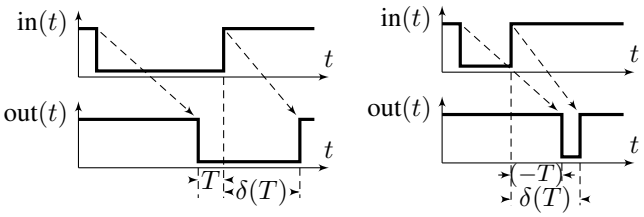

Figure 1: Left: Input/output signal of a single-history channel, involving the previous-output-to-input delay T and the resulting input-to-output delay $\delta(T)$. Right: Input transition with $T < 0$.

which are based on detailed analog models [44, 57, 17] of all elements of a digital standard-cell library. Since simulation times, e.g. using Spice [54], for even moderately complex circuits are prohibitively large, however, digital timing analysis/simulation tools such as Mentor Graphics ModelSim, Cadence NC-Sim or Synopsis VCS offer a much faster alternative. They are based on discrete-value (typically binary) circuit models augmented by *continuous* gate and wire delays. Like for static timing analysis, delay estimates are often obtained by means of elaborate timing prediction models like CCSM [40] and ECSM [62], which characterize the delay of a cell via (typically manufacturer-supplied) technology data, for example, tabulated input/output current waveforms for varying parameters such as input slew rate and output capacitive load [61]. These delay estimates are used to parametrize pure or inertial[4] delay [63] channels in a binary-value, continuous-time circuit model of a given circuit, instantiated e.g. as VHDL-Vital or Verilog timing libraries, which are employed in subsequent simulation and dynamic timing analysis runs.

It is apparent, however, that pre-computed pure or inertial delays are constants, i.e., remain the same throughout these runs. More accurate results can be expected from channels with non-constant delays, which are mandatory for properly modeling time-variant phenomenons such as decaying glitch trains. In [31], we introduced the notion of single-history channels, which are characterized by a delay function $\delta(T)$ that depends on a parameter T: As shown in Fig. 1, it maps a transition occurring at the channel input at time t to its corresponding output transition at time $t + \delta(T)$, where T is the input-to-previous-output delay. Single-history channels not only allow to model decaying pulse propagation, but also vanishing pulses: If two succeeding input transitions would, according to $\delta(T)$, occur at the output in reversed order, they cancel each other. Furthermore, single-history channels allow for different rising and falling transition delays, specified by two delay functions $\delta_\uparrow$ and $\delta_\downarrow$, respectively.

Quite unexpectedly, we were able to prove in [31] that no *bounded* single-history channel (where the delay functions are upper- and lower-bounded) are realistic (not to speak of faithful): For the simple *short-pulse filtration* problem (SPF), which is essentially the problem of building a one-shot inertial[5] delay, we showed that pure (= constant) delay channels do not allow to solve SPF with unbounded stabilization time, whereas bounded single-history channels with non-constant delays, including inertial delay channels [63] and the more advanced DDM channels introduced by Bellido-Diaz et. al. in [7, 8], allow to design circuits that solve bounded SPF. Since this contradicts reality, in particular, the inability of a bistable circuit to recover from a metastable upset in bounded time, as established by Marino [48], no binary circuit model based on bounded single-history channels can be realistic.

In [30], we eventually succeeded to introduce a new class of single-history channels with *unbounded*

[4]A pure delay channel just delays an arbitrary input signal by a fixed time delay, an inertial delay channel does the same but suppresses signal transitions that are closer than some minimum time to each other.

[5]What we mean by inertial delay is a single-input-single-output component that propagates an input pulse only if it is longer than some minimum duration, and completely suppresses it otherwise.

delay functions, called *involution channels*, with the distinguishing property of having (negative) delay functions that are mathematical involutions, i.e., $-\delta(T)$ must form its own inverse. Besides proving mathematically that they are realistic w.r.t. the SPF problem, our experimental evaluation in [56] demonstrated a reasonable accuracy of the predictions of the involution model for a simple real circuit, namely, an inverter chain as well. Therefore, to the best of our knowledge, a binary circuit model based on our involution channels is the only candidate for a faithful model known so far. Finally, in [29], which earned a nomination for the best paper at DATE'18, we were able to show that the involution model remains faithful even in the presence of a certain amount of (adversarially generated) noise.

The proposed project shall start out from these very encouraging results, in an attempt to systematically explore and enlarge the modeling power of the involution model and variants thereof. In particular, we will address the following major open scientific questions:

(1) The existing involution model has limitations that must be addressed in order to arrive at a model that is not only faithful for the SPF problem, but rather for a substantially large class of circuits. Besides the principal insufficiency of a scalar-valued delay function to cover phenomenons like ringing, where a single input transition may cause multiple output transitions, it does not allow composition of gates with different electrical characteristics (in particular, threshold voltages), and does not support bandwidth-limited interconnects either. Developing a sound theoretical basis for how to compose realistic models in a way that leads to a realistic model of the compound circuit is not only scientifically challenging, but also a mandatory prerequisite for making the involution model practically relevant.

(2) The existing involution model does not allow to incorporate subtle delay variations in the case of multi-input gates. In particular, it is well-known that the gate delay of a, say, 2-input NAND gate, measured from the falling output transition to the later of the two rising input transitions, also depends slightly on the time difference between the two rising input transitions. This dependency is called the *Charlie effect* [21], and originates in the series/parallel composition of the transistors in the stacks of a multi-input CMOS gate. In order to accurately model circuits [34] that exploit the Charlie effect, it is absolutely mandatory to have a delay model that also covers this subtle effect appropriately.

(3) It is not at all clear how to determine $\delta_\uparrow(T)$ and $\delta_\downarrow(T)$ for a real gate in practice, except via explicit delay measurements. These, however, are infeasible for actual circuits in practice, given the wide variety of operating conditions (load, supply voltage) the very same gate may experience at different placements. Whereas this information could in principle be obtained by analog simulations, this suffers again from excessive simulation times. Moreover, detailed analog models for every single gate, for every transitor sizing, as well as post-layout information are of course mandatory for this purpose. What we are looking for instead are solid foundations for the direct characterization of the delay functions of real gates, ideally parametrized by only few model parameters, similar to what has been done for the (unfortunately not realistic) DDM model in [1, 41, 52]. Developing such a characterization requires the analysis of the transistor models of digital circuits, which can be described by systems of differential equations [45] and explored by means of analog simulations, for example.

(4) The modeling accuracy of the variants of the involution model to be developed in (1)–(3), like of

any alternative bounded single-history channel model, may be insufficient for certain applications. An obvious research challenge is to look for further generalizations of the model. Besides capturing modeling inaccuracy by a further relaxation of the adversarial noise model of [29], we have identified several possible avenues here: First, the existing model completely discards canceled transitions, which boils down to throwing away information on the underlying analog waveform that could be utilized in a generalized model. A natural further generalization are *multi-history channels*, where the delay of a transition depends not only on the time of the previous output transition, but, say, also on the time of the last-but-one output transition. An alternative for the latter could be to add information on the *slope* of the underlying analog signal to the binary abstraction.

In addition to this foundational work, we will also take some first steps towards incorporating our model into existing timing analysis (ModelSim) and verification (C2E2 [23]) tools, which will demonstrate its practical feasibility and allow us to experimentally evaluate its accuracy.

In summary, DMAC will explore an up to now almost completely uncharted territory in the field of modeling and analysis of digital integrated circuits. Thanks to our extremely encouraging first results obtained in some past research projects, and the already proven research competence of the primary project members and the external collaborators Matthias Függer (ENS Paris-Saclay), Thomas Nowak (Université Paris-Sud), Sayan Mitra (U. Illinois at Urbana-Champaign), Laura Nenzi (U. of Trieste) and Ezio Bartocci (TU Wien), we are convinced that DMAC will be most successful.

1.2 State of the Art

Whereas there is a wealth of research devoted to the analog modeling of digital circuits (see [54, 39, 44, 57, 17] for a few references), to the best of our knowledge, the issue of building digital abstractions atop of it and studying the solvability of problems in the resulting model has never been reconsidered after some ground-breaking work decades ago, with the notable exception of the work related to ternary simulations of digital circuits [50, 11, 46].

In fact, digital circuit models have been proposed as a general approach for modeling asynchronous circuits already by Unger in 1971 [63], where he proposed a general technique for deriving asynchronous sequential switching circuits that can cope with unrelated input signals. The model assumes signals to be binary valued, and requires the availability of combinational circuit elements, as well as pure and inertial delay channels. These models have been heavily used both in research and in industrial timing simulators since then.

In 1977, Marino [48] showed that the problem of building a synchronizer can be reduced to the problem of building an inertial delay channel. The reduction circuit only makes use of combinational gates and pure delay channels in addition to inertial delay channels. Marino further showed, in a continuous-value signal model, that for a set of standard designs of inertial delay channels, input pulses exist that produce outputs violating the requirements of inertial delay channels. Barros and Johnson [3] extended this work, by showing the equivalence of arbiter, synchronizer, latch, and inertial delay channels.

Marino [47] also developed a general comprehensive theory of metastable operation, and provided impossibility proofs for metastability-free synchronizers and arbiter circuits for several continuous-value circuit models. Branicky [9] proved the impossibility to construct a time unbounded, deterministic and time-invariant arbiter in an ordinary differential equations model. In a model based on continuous automata, this was studied by Mendler and Stroup [51].

Brzozowski and Ebergen [10] formally proved that, in a model that uses only binary values, it is impossible to implement Muller C-Elements (among other basic state-holding components used in (quasi) delay-insensitive designs) using only zero-time logical gates interconnected by wires without timing restrictions.

Bellido-Díaz et al. [8] proposed the PID model, and justified its appropriateness both analytically and by comparing model predictions against Spice simulations. The results confirm very good accuracy even for such challenging scenarios as long chains of gates and ring oscillators. In [41], the PID model (later renamed to Delay Degradation Model DDM) was generalized from inverters to (N)AND and (N)OR gates. Thanks to considerable efforts like [52, 41] spent on the question of how to extract the DDM model parameters from technology parameters, the DDM model has already made its way into digital timing analysis tools [7].

Michael Mendler et. al. [50] introduced *up-bounded non-intertial* (UN) channels as the core part of a model for *constructive* circuits. They further relaxed the *up-bounded inertial* (UI) channels [11], which in turn relaxed classic inertial delay channels by allowing an unstable output for a bounded amount D of time after an input signal transition. UI channels have been used primarily in conjunction with ternary simulations (where in addition to logical 0 and 1 a third state X is present) [46]. Unlike classic inertial delay channels, both UI and UN channels allow arbitrary short pulses, i.e., arbitrarily close transitions, at the output. However, whereas UI channels stipulate some relation between the output and the previous input also for times shorter than D, this requirement has been dropped for the UN channels. Consequently, UN channels may show completely arbitrary output behavior during D time after an input signal transition.

In [50], it has been shown that *UN logic*, which provides a modal D-bounded stabilization operator, provides an adequate basis for the axiomatic specification of circuits based on UN channels and their ternary simulations. Unlike in classic ternary simulation based on UI channels, however, where X has an unclear semantics, X stands for "oscillation" in the UN model. A key property of the resulting constructive circuits is that if a circuit stabilizes at all, it does so in bounded-time and to a *unique* output value, in all executions.

It is apparent that this clear dichotomy between oscillation forever and bounded-time unique stabilization is not always realistic in our sense, as there are real circuits with unbounded stabilization times und non-unique output values. This is in accordance with our findings, since involution channels are more restrictive than UN channels: they do not allow arbitrary unstable behavior within D time, so may prohibit perpetual oscillation in some situations, resulting in finite but unbounded stabilization times.

1.2.1 Related own results

In [30], we introduced our involution channels, the only realistic candidate model known so far, and demonstrated in [56] that it allows to reasonably accurately model an inverter chain. We note that the latter work used both elaborate Spice simulations as well as real measurements of a custom ASIC [38], where an inverter chain has been instrumented with very high-bandwidth analog amplifiers that allow to directly connect the 50 Ω input of a real-time oscilloscope to any stage. Note that this ASIC, as well as some successors, have been developed in the context of our past FWF project FATAL[6] devoted to radiation-

[6]FATAL (P21994) was a joint project of our group and the group of Horst Zimmermann at the Institute of Electrodynamics, Microwave and Circuit Engineering at TU Wien. It has been continued later on in another joint FWF project EASET (P26435) led by Andreas Steininger, which produced, among other results [59, 64], ASICs instrumented by improved analog amplifiers [53].

induced single-event transients in digital circuits, and are of course available for further experiments.

Like every *deterministic* delay model, however, the involution model necessarily has limited modeling power: many different effects in physical circuits cause various types of noise in signal waveforms and, hence, *jitter* in the digital abstraction [12]. No deterministic delay function can properly capture the resulting variability in the signal traces. In [30], we managed to relax the involution model by adding limited *non-determinism* on top of the (deterministic) involution delay function $\delta(T)$. We proved that this can be done without sacrificing faithfulness: both the original SPF impossibility result and, in particular, a novel SPF possibility hold for this generalized model, provided the maximum jitter is small enough.

Note that adding non-determinism is a convenient way of securing maximum generality: no practically observable bounded jitter phenomenon, neither bounded random noise, from white to slowly varying flicker noise [12], nor even *adversarially* chosen transition time variations can invalidate the faithfulness of the resulting $\boldsymbol{\eta}$*-involution model*. Deterministic effects, like slightly different thresholds due to process variations, are also covered to some extent. The latter is particularly interesting for the proposed project, as interfacing circuits with different electrical characteristics might be covered this way. Unfortunately, however, the results of [30] do not allow to extend the impossibility results to deterministic effects. In fact, it may turn out that deterministic delay variations may cause the impossibility result to break.

1.2.2 Not directely related work

Below, we will provide some references on research in areas, which are not directly related to the work to be done in the proposed project, but need to be added in order to establish the proper context.

Fault tolerant circuits. Our interest in binary models that faithfully model glitch propagation and even metastability has been stimulated by the increasing importance of incorporating fault-tolerance in circuit design [14], which gave rise to the research projects FATAL, EASET and SIC conducted at our group: Reduced voltage swings and smaller critical charges make circuits more susceptible to particle hits, crosstalk, and electromagnetic interference [33, 49]. Since single-event transients, caused by an ionized particle hitting a reverse-biased transistor, just manifest themselves as short glitches, accurate propagation models are important for assessing soft error rates, in particular, for asynchronous circuits. After all, if system-level fault-tolerance techniques like triple modular redundancy are used for transparently masking value failures, the only remaining issue are timing failures, among which glitches are the most problematic ones.

For example, our Byzantine fault-tolerant distributed clock generation approach DARTS [32] makes use of standard asynchronous circuit components, for example micropipelines [60], which store clock ticks received from other nodes; a new clock tick is generated when sufficiently many micropipelines are non-empty. Clearly, since any "wait-for-all" mechanism may deadlock in the presence of faulty components, handshaking had to be replaced by threshold logic in conjunction with some bounded delay assumptions. This way, DARTS can tolerate arbitrary behavior of Byzantine faulty nodes, except for the generation of pulses with a duration that drive the Muller C-elements of a pipeline into metastability. Analyzing the propagation of such pulses along a pipeline is thus important in order to assess the achievable resilience against such threats [28]. The situation is even worse in case of self-stabilizing algorithms [20], which must be able to recover from an arbitrary initial/error state: Neither handshaking nor any bounded delay condition can be resorted to during stabilization in an algorithm like our self-stabilizing, Byzantine fault-tolerant FATAL clock generation scheme [18, 19]. Consequently, glitches and the possibility of

metastability cannot be avoided.

As a consequence, discrete-value circuit models, analysis techniques and supporting tools for a fast but nevertheless accurate glitch and metastability propagation analysis will be a key issue in the design of future robust VLSI circuits. Note carefully that, despite their conceptual simplicity and methodological completeness, constructive circuits and UN logic [50] are too restrictive for modeling self-stabilizing fault-tolerant circuits. Searching for faithful models hence remains an important challenge for future research on asynchronous fault-tolerant circuits.

Simulation and verification of hybrid systems. Analog and mixed-signal circuits have provided a well-spring of hard problem instances for formal verification of hybrid systems (HS). Tools like HyTech [37], PHAVer [26], SpaceEx [27], Checkmate [36], d/dt [15], and Coho [65] have targeted and successfully verified linear dynamical and hybrid models for tunnel-diode oscillators [43], $\Delta\Sigma$ modulators [36, 15], filtered oscillators [27], and digital arbiters [65].

However, realistic circuit models are (highly) non-linear, which makes linear models questionable in general, and causes the linear approximation-based methods to be too conservative. Only recently, verification tools such as Flow* [13], NLTOOLBOX [16], iSAT [25], dReach [42], C2E2 [23] and CORA [2], have demonstrated the feasibility of verifying nonlinear dynamic and hybrid models. These tools are still limited in terms of the complexity of the models and the type of external inputs they can handle, and they require quite often manual tuning of algorithmic parameters.

The verification challenge for nonlinear circuits is further exacerbated by the fact that these problems often require state exploration in regions, where the model is very sensitive. For example, bi-stable circuits like a storage element or a flip-flop can be driven into a metastable state where the circuit may output signals in the forbidden region between logical 0 and logical 1 or experience very high-frequency oscillations for an arbitrary time, before resolving to a proper state [47]. In a joint work [22] with Sayan Mitra's group at the University of Illinois at Urbana-Champaign and Ezio Bartocci from our institute, conducted in the RiSE/SHiNE project, we presented a novel discrepancy-function-based technique for verifying nonlinear dynamic and hybrid models with externally controlled input functions using the C2E2 tool [23]. It combines numerical simulation with model-based sensitivity analysis for bounded invariant verification, and has been used for exploring metastability in bi-stable circuits like a fed-back OR-gate. It revealed interesting insights into the close connection between sensitivity and metastability recovery time.

The hybrid simulation and verification tools developed in the above research provide a rich basis for experimentally validating the delay models to be developed in the proposed project: Thanks to our involvement in the verification of digital circuits using C2E2 [22], which rests on a promising uniform transistor model [45] for CMOS devices, we have a very powerful tool at our disposal, which not only facilitates simulation but also simulation-driven verification of digital CMOS circuits driven by arbitrary input waveforms, including Sigmoids.

1.3 General Methodological Approach

In order to accomplish the scientific goals (1)-(4) already outlined in Section 1.1, the actual work in DMAC will be partitioned into two well-defined and reasonably independent tasks:

(1) **Task 1: Guaranteeing Faithfulness of the Involution Model** [(1),(2)]

Model composition; multi-input gates; generalized adversarial noise.

(2) **Task 2: Gate Characterization and Model Generalization** [(3),(4)]

Characterization of gates; multi-history channels; Sigmoidal waveforms.

As both tasks have a clear focus and also require somewhat specific skills, they shall be performed by two different PhD students.

1.3.1 Task 1: Guaranteeing Faithfulness of the Involution Model

Start	Duration	Responsible persons
$T0$	4 years	NN1 (PhD student), Ulrich Schmid

Start	Duration	Responsible persons
$T0 + 12$	1 year	2 Master students M1, M2, 6 months 20h/week each

Challenge (1). The existing involution model, which is appealing due to its simplicity, has several limitations that severely impair its faithfulness. Most importantly, whereas it has been proved already [30] that the model is realistic for the SPF problem, the fundamental question whether it is realistic also for other problems is widely open.

Besides this basic issue, there are also other limitations. The arguably most severe one is that the existing involution model lacks compositionality, except for the case where all gates have identical electrical characteristics (in particular, threshold voltages) and where all interconnects consist of pure wires (no bandwidth limitations). In order to arrive at a faithful circuit model, we need a variant of involution channels that facilitate gates with different threshold voltages and bandwidth-limited interconnects. Moreover, in modern high-speed circuits, there are phenomenons like ringing, i.e., decaying oscillation caused by the inevitable inductances in wires and transistors, where a single input transition at a gate may cause several consecutive output transitions. As this is inherently incompatible with modeling delays as a scalar-valued function, the existing involution model must be extended appropriately.

In addition, we will consider ways to improve the modeling coverage of the existing involution model. The adversarial noise model of [29] was already a first step into this direction, which addressed the obvious problem that a deterministic delay function cannot capture stochastic delay variations, for example. Unfortunately, however, tight restrictions on the maximum delay variation in [29] severely limit the model coverage w.r.t. real circuits.

Challenge (2). The existing involution model does not allow to accurately model the delay of multi-input gates. It is well-known that the delay of a, say, 2-input NAND gate, measured from the falling output transition to the later of the two rising input transitions, also depends (slightly) on the time difference between the two rising input transitions. This Charlie effect [21] originates from the series/parallel composition of the transistors in the stacks of a multi-input CMOS gate. In order to accurately model circuits like the ring oscillator described in [34] that exploits the Charlie effect, it is absolutely mandatory to have a delay model that also covers this subtle effect appropriately.

Unfortunately, naive approaches to apply the original involution model to multi-input gates do not allow this: Combining the output of multiple single-input-single-output involution channels via zero-time boolean functions, the only available elements besides channels in the current model, cannot affect delays in the way needed for modeling the Charlie effect. What is needed here is a true multi-input involution channel, and the central question is how to define its delay function $\delta(.)$. Oviously, for a two-input gate, $\delta(T_1, T_2)$ now depends on (at least) two parameters, but how? Is there a natural generalization of the involution property that is compatible with the Charlie effect?

Starting points for Task 1.

- *Problem reductions for going beyond SPF*

  In order to extend the range of problems where the involution model and its variants are still realistic, reductions are a simple and elegant way: If one can show that some problem X can be reduced to SPF, i.e., solved if a solution for SPF is available, and vice versa, it follows that the model is also realistic w.r.t. problem X. However, since SPF is a very simple problem, it is very likely that we will need also novel impossibility proofs and implementations dedicated to stronger "canonical" problems Y in order to prove that some circuit model is realistic also for Y.

- *Using a 2-threshold model*

  The simple analog switching waveform model [30] (see the description of Task 2 below for a short introduction) of a channel that leads to involution delays uses a fixed threshold voltage level for both rising and falling transitions. One natural generalization would be an analog model that uses different threshold voltages here. This would not only better match reality, where e.g. one usually observes different threshold voltages for characterizing the mode switches of pMOS and nMOS transistors [45], but might also contribute to decreasing some currently uncovered dependency of delays on switching waveforms. Most importantly, however, it might add another degree of freedom in attempts to matching different threshold voltages of successive gates via a special type of interconnecting channels.

- *T-dependent adversarial noise*

  In the existing adversarial noise model of [29], the adversary may change every output signal transition by some time chosen arbitrarily in a fixed interval $[-\eta^-, \eta^+]$. However, the interval boundaries are constants and actually depend on the delay function in a non-trivial way. One promising idea is to make $[-\eta^-, \eta^+]$ for an output transition, originally delayed by $\delta(T)$, dependent on T. We expect that this will considerably increase the ability of the resulting model to capture the behavior of real circuits, without the need to change the underlying involution model.

- *Vector-valued delay functions*

  In order to cope with ringing signals, generalizing $\delta(T)$ to a vector-valued function (that provides the delays for all subsequent ringing output transitions) comes to mind. We may also get some inspiration from analyzing the essential differences of UI channels [11] and UN channels [50], which both allow such behavior.

- *Simulation studies of real circuits for building hypotheses*

  Using Spice simulations of real 2-input gates and/or C2E2 simulations of suitable transistor models, we can experimentally determine how $\delta(T_1, T_2)$ looks like. For the Charlie effect, one possible hypothesis would be that, for a fixed difference $\Delta = T_1 - T_2$, the resulting one-parameter delay function $\delta(\Delta, T_2)$ is an involution w.r.t. T_2. Alternatively, higher-dimensional involutions [58] may turn out to fit the empirical data. Our hope is that these experiments will eventually lead to a hypothesis (like our switching waveform model) that explains the observations in a satisfactory way. In addition, we will of course use such experiments for validating any candidate hypothesis.

Major outcomes and required skills. The main focus of Task 1 will be on theoretical results, i.e., suitable definitions of generalized delay functions and formal-mathematical proofs of the resulting models being realistic for a larger class of problems. Recall that, right now, we only know that the involution model is realistic w.r.t. the SPF problem. Besides reductions, where one needs to show that certain problems are equivalent w.r.t. solvability to SPF, this may need novel impossibility proofs and implementations dedicated to canonical problems other than SPF. This part of the work requires typical computer science skills (abstraction, formal-mathematical analysis, correctness and impossibility proofs).

Besides theoretical results, Task 1 also involves some experimental work, in particular, Spice as well as C2E2 simulation and verification runs (which will be supported, and partially be taken over, by our external collaborator Sayan Mitra) for the development of suitable hypotheses for the modeling and for accuracy validation. Key data used in scientific publications will of course be made accessible publicly, following the open access policy of the FWF. In the course of this experimental work, we also hope to stimulate some further developments of C2E2. In more detail, our joint work [22] led to the introduction of "thin variables" in C2E2, which allowed to incorporate arbitrary input signals without undue bloating. Our adversarial noise model [29] might raise sufficient interest for implementing "thick variables" in C2E2, which would allow to incorporate arbitrary input signals with noise.

Last but not least, Task 1 will also require some implementation work devoted to making our results accessible also in practice. More specifically, we will incorporate our delay model in ModelSim, which is relatively easy as its basic mechanisms already support the cancellation of out-of-sequence signal transitions. This step is mandatory, since we will not be able to publish papers devoted to a new digital circuit model at VLSI conferences without being able to compare our model predictions with the ones obtained by existing dynamic timing analysis techniques. All this implementation work will be primarily delegated to Master students M1 and M2 working towards their theses. Note that splitting this work on two Master students is necessary, since we expect our model to develop significantly over time, which requires also matching implementations that cannot be maintained by a single Master student within the avaliable time frame (6 months).

All the other work in Task 1 will be conducted by a PhD student (NN1) working towards his thesis, under the supervision of the project leader Ulrich Schmid. The required skills perfectly match graduates from the Bachelor + Master program "Computer Engineering" at TU Wien, or similar international computer science of computer engineering programs.

Principal work plan. From a research perspective, Task 1 is ideal since its research challenges (1) and (2) are essentially independent of each other. Within each challenge, there is a natural serialization:

(1) Perform simulations for building candidate hypotheses.

(2) For every chosen candidate hypothesis:

- Formalize it mathematically.
- Analyze its properties.
- Implement it in ModelSim and validate the modeling accuracy using simulations.

(3) Integrate it in a comprehensive digital circuit model and evaluate its accuracy for some larger application(s).

Collaborations. The work in Task 1 will be supported by the following external collaborators:

- *Matthias Függer* (ENS Paris-Saclay), who will contribute to the formal-mathematical proofs and the accuracy evaluation experiments.
- *Thomas Nowak* (Université Paris-Sud), who is an expert in advanced mathematical proofs.
- *Sayan Mitra* (U. of Illinois at Urbana-Champaign), who will provide expertise and actively contribute to C2E2-based simulations.

To support our joint work, we foresee additional financial support for two 1-month research visits of NN1 in Paris (EUR 4.000,– each) and one at Urbana-Champaign (EUR 5.000,–). Naturally, it is difficult to assess now when these visits will take place, as this depends not only on the progress made in the project but also on the availability of the collaboration partners. However, we expect the former two visits to happen in the first and second (or third?) year, as they are primarily devoted to advancing the existing model. The visit at Urbana-Champaign is likely to happen in the second year, when the need for more refined simulation validation arises.

To support Master students helping us with implementations and experimental work, we foresee two positions M1 and M2 (6 months, 20h/week each).

1.3.2 Task 2: Gate Characterization and Model Generalization

Start	Duration	Responsible persons
$T0$	4 years	Jürgen Maier (PhD student), Andreas Steininger

Start	Duration	Responsible persons
$T0 + 12$	1 year	2 Master students M3, M4, 6 months 20h/week each

Challenge (3). A crucial problem for every model, hence also the involution model, is parametrization: The existing involution model is in fact "parametrized" via the delay functions $\delta_\uparrow(T)$ and $\delta_\downarrow(T)$, and the core question is hence: How does one determine these functions, which are far from being static even for a given gate in a given technology with given transistor sizing: delays depend heavily on the output load and the supply voltage, and even on the electrical characteristics of the interconnect and the subsequent gate, recall Challenge (1). Unlike existing delay prediction models like CCSM [40] and ECSM [62], which characterize the delay of a gate via (typically manufacturer-supplied) technology data, we need more than just tabulated input/output current waveforms for varying parameters such as input slew rate and output capacitive load [61]: We need a family of mathematical involutions, i.e., analytic functions that accurately describe the delay of the gate depending on T, which can be parameterized to express the dependency on load and supply voltage.

Challenge (4). The second main challenge to be addressed in Task 2 are generalizations of single-history involution channels, with the purpose to increase the modeling accuracy. A very natural idea is to also make use of canceled transitions, which are just discarded in the existing model. Still, canceled transitions provide useful information about the behavior of the underlying analog waveform *between* signal transitions, which can be utilized to increase the accuracy of the model predictions.

A natural idea for further improving accuracy is to generalize single-history to multi-history single-input-single-output channels. In the case of 2-history channels, for example, the delay function $\delta(T_1, T_2)$ would depend on two parameters, this time related to the time difference T_1 between the current input transition and the last output transition, and the difference T_2 between the current input transition and the last-but-one output transition. Like for the Charlie effect, the central question is again what the properties

of the resulting $\delta(T_1, T_2)$ are. Is there a natural generalization of the existing involution property? Is there a simple analog model that leads to the resulting multi-history delay function?

An alternative idea for improving the accuracy of the current involution model is to extend the current discrete-value continuous-time model, which can be viewed as being based on Heaviside signals: A quite natural idea is to generalize the basic model to an abstraction that also incorporates information on the *slope* of the underlying waveforms. In particular, we will consider replacing Heaviside signals by Sigmoidal ones and study the resulting abstraction.

Starting points for Task 2.

- *Schematics-based gate characterization*

  A natural approach for developing hypotheses for the delay functions is to start out from the transistor-level schematics of the gates, and to use suitably simplified transistor models for explaining the shape and, most importantly, characteristic parameters of the switching waveforms. From this, as outlined below (Generalizing from the switching waveform abstraction), one may infer shape and parameters of the corresponding delay functions. A particular attractive prospect of this approach lies in the fact that a successful characterization would automatically allow us to quantitatively incorporate the effect of parameter variations (both process parameters and electrical ones) on the delay functions.

  In some previous work, we have developed a uniform transistor model [45] and also a hybrid transistor model, which can be simulated using C2E2 [22] (see below) and hence provide excellent starting points for this work.

- *Using information from cancelled transitions*

  The existing involution model completely drops canceled transitions. The switching waveform abstraction outlined above reveals, however, that canceled transitions actually correspond to pulses (= two consecutive rising/falling transitions), which do not reach the threshold voltage and hence remain "invisible" in the digital abstraction. A natural idea is to use some of this information to increase the accuracy of a generalized model. Using *all* this information would boil down to a complete "encoding" of the analog waveform, resulting in a model that is almost as expensive as a fully-fledged analog model. Moreover, using the resulting channels in feedback loops would create troubles w.r.t. uniqueness/computability of traces in the resulting model. However, there may be ways to use only *some* of the information of canceled transitions.

- *Generalizing from the switching waveform abstraction.*

  In [30], we showed that there is a simple analog model of a circuit that naturally leads to involution delay functions. It is based on a pair of arbitrary but continuous rising and falling switching waveforms (exponentials, i.e., solutions of a first-order ordinary differential equation in the simplest case), which are triggered by the respective rising and falling input Heaviside jump. If they are joined in a way that ensures continuity of the output waveform caused by an arbitrary input trace, then the corresponding delay function satisfies the involution property. In a way, this model shows that there is some non-trivial relation between switching waveforms and delays.

  It may be possible to generalize this model to both multi-input gates and multi-history delay functions, and get inspiration of the resulting properties of the delay function corresponding to this

generalized model. In the case of 2-history delay functions, for example, we expect the corresponding model to be some 2nd-order system. Note also that there are alternatives to just pasting together rising and falling switching waveforms to get a continuous overall waveform: adding them may also do the job (the latter is particularly promising for the possible generalization of Heaviside signals to Sigmoids).

- *Simulation studies of real circuits for building hypotheses*

  Using Spice simulations of real gates, we can also experimentally determine how the 2-history delay function $\delta(T_1, T_2)$ looks like. Does it match higher-dimensional involutions [58]? Our hope is that such experiments will eventually lead to a hypothesis (like our switching waveform model) that explains the observations in a reasonably satisfactory way. In addition, we will of course use such experiments for validating any hypothesis we will arrive at.

- *Sigmoidal waveforms*

  In a recent collaboration [22] with Sayan Mitra, Ezio Bartocci and Laura Nenzi in the context of RiSE/SHiNE, we developed an idea of how to generalize the Heaviside signals inherently underlying the discrete-value involution model by parameterized Sigmoid waveforms. Initial experimental studies conducted by Laura Nenzi and Jürgen Maier in the context of the RiSE/SHiNE project revealed that pulses can be accurately expressed by adding shifted Sigmoids. An exciting question is whether one can build a generalized involution model based on this abstraction.

Major outcomes and required skills. The main focus of Task 2 will be on finding abstractions facilitating accurate delay modeling for real integrated circuits, and finding approaches for defining and determining characteristic parameters. Envisioned outcomes are appropriately parameterized delay functions and methods for determining the parameters for a given technology. This work requires expertise in understanding transistor-level schematics and analyzing the corresponding models, with are usually systems of *ordinary differential equations* (ODEs). Hybrid models, comprising multiple ODE models enabled by discrete mode switches that can e.g. be used for accurately describing the behavior of CMOS transistors in different operation regions [45], may also be considered.

Besides this foundational and analytic work, Task 2 also involves an experimental part, in particular, Spice as well as C2E2 simulation and verification runs, and possibly even measurements, for gate characterization and accuracy validation. Key experimental data used in scientific publications will of course be made accessible publicly, following the open access policy of the FWF. The hardware and software required for conducting these experiments is locally available at our group; specific electrical engineering expertise will be provided by Andreas Steininger, of course. Should the need for expensive measurement equipment arise, we can rely on our collaboration partners (in particular, the group of Horst Zimmermann at the Institute of Electrodynamics, Microwave and Circuit Engineering) in the Faculty of Electrical Engineering and Information Technology at TU Wien.

Like for Task 1, we also expect some implementation work in Task 2, which can be delegated to Master students M3 and M4 working towards their theses. Besides developing experimental testbeds for various simulation and possibly measurement experiments, to be developed by M3, we will also need a tool that allows us to automatically generate compound ODE models for a given sample circuit design, based on the ODE models of the gates. Among the challenges faced by M4 is the need to support specification languages that can be processed immediately by verification tools like C2E2 and others.

The research profile required for Task 2 requires a PhD student (Jürgen Maier) working towards his thesis, under the co-supervision of Andreas Steininger and the project leader Ulrich Schmid. The required skills are perfectly matched a graduate from both the Electrical Engineering and Computer Engineering Master programs at TU Wien like Jürgen Maier, who did already contribute to some earlier publications [29, 22] directly related to DMAC.

Principal work plan. From a research perspective, Task 2 is again ideal since its research challenges (3) and (4) are independent of each other. The natural serialization of the work for (3) is as follows:

(1) Study transistor-level schematics and their corresponding ODE models, both analytically and by means of Spice or C2E2 simulations, for building candidate hypotheses.

(2) Design systematic validation experiments for validating hypotheses against the behaviors of real circuits (Spice simulations, possibly measurements)

(3) For every chosen candidate hypothesis, run validation experiments.

The research work for challenge (4) will involve some interaction with Task 1, in the sense that the effect of modeling choices w.r.t. faithfulness of the resulting generalized model need to be verified. This part is hence likely to stimulate some truly joint work. Nevertheless, this only concerns the question of whether a generalized modes remains realistic; the accuracy validation part is entirely within Task 2 and follows the pattern (1)–(3) sketched above.

Collaborations. The work in Task 2 will be supported by the following external collaborators:

- *Sayan Mitra* (U. of Illinois at Urbana-Champaign), who will provide expertise and actively contribute to C2E2-based simulation and verification.
- *Laura Nenzi* (U. Trieste) and Ezio Bartocci (TU Wien), who are experts in ODE models and hybrid systems [5, 4, 6, 35], will support our work on a Sigmoid-based generalized circuit model.

To support our joint work, we foresee additional financial support for a 1-month research visit in Trieste (EUR 4.000,–) and two at Urbana-Champaign (EUR 5.000,– each). Again, it is difficult to assess now when these visits will take place, as this depends on the progress made in the project and on the availability of the collaboration partners. However, we expect the former visit to happen in the third year, as it is primarily devoted to the envisoned Sigmoidal extension of our model. The two visits at Urbana-Champaign are likely to happen in the first and second year, as the work in Task 2 will very likely require refined simulation and verification runs that possibly even need some extension of C2E2.

To support Master students helping us with experimental work, we foresee two positions (6 months, 20h/week each).

2 Organizational Aspects

2.1 Institution: Institute of Computer Engineering (E191), TU Wien

Our research[7] is devoted to all aspects of the direct interaction of computer systems and their environment, from the lowest level of circuit and hardware architectures to safety-critical cyber-physical systems like industrial automation & smart grids, healthcare, spacecraft, and automotive.

[7] See https://ti.tuwien.ac.at/institute/research

Key characteristics of our research are hence (1) an *integrative view* of a multitude of system aspects, including hardware architectures, continuous/discrete systems, parallelism and communication, dependability, real-time processing, low-power design, energy and resource efficiency, decision and control theory, autonomy, etc., and (2) *interdisciplinarity*: Core computer science knowledge and skills like concurrent programming, modeling, design and analysis, formal verification and synthesis of both software and hardware are complemented by specific knowledge and skills from other disciplines, in particular, continuous mathematics, system theory and electrical engineering. Main research topics are digital circuits and hardware architectures, parallel and distributed, dependable, real-time systems, hybrid systems and optimal control, quantitative and runtime verification, computational modeling and simulation, autonomous systems, robotics and automation systems integration, and cyber-physical social systems & Internet of Things.

With respect to teaching, the Institute of Computer Engineering runs a Master and Bachelor program "Technische Informatik", which offer a thorough scientific and engineering education in the field of dependable embedded systems and hybrid systems.

The work in DMAC will be conducted by the institute's *Embedded Computing Systems* (ECS) group (E191-02). Its scope of the research and teaching activities ranges from dependable and power-efficient digital circuits to future generation computer architectures to networked embedded systems and fault-tolerant distributed systems in general. Nonwithstanding a clear focus on scientific research, the spectrum of our work ranges from formal-mathematical analysis to simulation-based experimental evaluation to prototype implementations. The ECS group consists of two full and one associate professor, namely, Ulrich Schmid (head, fault-tolerant distributed algorithms), Muhammad Shafique (future-generation computer architectures), Andreas Steininger (dependable digital circuits), six assistant professors, one secretary, and one technician. Rooms and infrastructure for the required additional project staff, as well as all equipment, are available. Needless to say, DMAC would contribute to secure (and hopefully increase) the existing reputation of our group.

2.2 Contributing Human Resources

- **Ulrich Schmid** is full professor and head of the Embedded Computing Systems Group since 2003. He authored and co-authored numerous papers in the field of theoretical and technical computer science and received several awards and prizes, like the Austrian START-prize 1996. Ulrich Schmid also spent several years in industrial electronics and embedded systems design. His current research interests focus on the mathematical analysis of fault-tolerant distributed algorithms and real-time systems, with special emphasis on their application in systems-on-chips and networked embedded systems. As DMAC lies in his major areas of interest, Ulrich Schmid will also actively contribute to the modeling activities and the impossibility/correctness proofs to be conducted in DMAC.

- **Jürgen Maier** is currently Universitätsassistent (30 h/week) at the Embedded Computing System Group at TU Wien since 2018. Previously he received Master's degrees both in Computer Engineering in 2014 and in Microelectronics and Photonics in 2016, both from TU Wien. His main research interests focus on transistor level circuit analysis and design and their implications on higher abstract quantities such as signal delays and metastability. In MADC he would be mainly responsible for Task 2. Due to his experience he will however also support the work in Task 1.

- **NN1**: We are still looking for a PhD student with computer engineering background.
- **M1 – M4**: We are still looking for 4 Master students (6 months, 20h/week) working on their thesis.
- **Andreas Steininger** is associate professor in the ECS group. He is an experienced hardware designer and project leader who has been involved in many national and international projects concerned with the design of fault tolerant digital circuits and their evaluation by means of fault injection. During his former 10 year employment at the Electrical Engineering Department he has gained experience in analog circuit design as well. His current research interests further include self-healing circuits and asynchronous design with a focus on robustness against parameter variations as well as fault effects.
- **Ezio Bartocci** is a tenure-track Assistant Professor at the Cyber-Physical Systems Group (E191-01) at the Institute of Computer Engineering of TU Wien. The primary focus of his research is to develop formal methods, computational tools and techniques that support the modeling and the automated analysis of complex computational systems, including software systems, cyber-physical systems and biological systems. On these topics he co-authored more than 80 referred papers published in the main international journals and top-tier conferences of his research areas (CAV, TACAS, ATVA, CDC, EMSOFT, HSCC, etc.), generating more than 1800 citations (h-index $\geq$ 26) according to Google Scholar.
- DMAC will also involve a number of external collaborations, in particular, **Matthias Függer** (ENS Paris-Saclay), **Sayan Mitra** (U. of Illinois at Urbana-Champaign), **Laura Nenzi** (U. Trieste), **Thomas Nowak** (Université Paris-Sud).

2.3 Required Other Costs

To support the external collaborations in DMAC, additional financial support for 3 x 1-month research visits in Europe (Paris, Trieste) (estimated total costs EUR 12.000,–) and 3 x 1-month research visits in USA (estimated total costs EUR 15.000,–) are foreseen. All the required equipment and infrastructure will be available, so there are no further additional costs.

3 Dissemination Strategy

As DMAC is a basic research project, dissemination of the project results will be primarily (i) via talks + scientific publications in good conferences in the field and (ii) via comprehensive journal publications in good scientific publication venues.

Following good scientific practice (and adhering to the open access policy of the FWF), key experimental data used in scientific publications will also be made publicly accessible. Moreover, we will also make our prototype implementations publicly usable, which is very important to allow other researchers to follow up on or relate to our results.

Last but not least, owing to the fact that our institute plays a leading role in the Bachelor and Master program “Technische Informatik” in the Faculty of Informatics at TU Wien, it is very much in our interest to incorporate the research conducted in DMAC into our lectures: Without such measures, it is impossible to attract the attention of good Master students for writing their theses in the context of the project (hence, to fill our respective positions M1–M4), and thus to educate future PhD students.

4 Expected Additional Benefits

Since we hope to improve the state-of-the-art in the hot area of dynamic timing analysis of digital circuits, we expect DMAC not only to improve the scientific state of the art in digital circuit modeling and analysis in general, but also to generate mid-term benefits for the industrial practice. Eventually, we therefore hope to also contribute to making future general digital electronics more dependable. Moreover, given the similarity of digital circuit modeling with biological circuit modeling [4, 6, 35], even cross-disciplinary benefits may eventually emerge from our research.

5 Ethical Aspects

For this project there are no ethical aspects to consider and there are no sensitive experiments planned. We mention, though, that our overall goal of improving the dependability of digital electronics contributes to mitigating the negative side-effects of the dependency of our society on computing systems.

A Abbreviations

Abbrev.	Description	Definition
ASIC	Application-Specific Integrated Circuit	Sect. 1.2.1
CMOS	Complementary metal-oxide semiconductor	Sect. 1.2.2
DDM	Delay Degradation Model	Sect. 1.2
EASET	FWF P26435: Accelerator-based Experimental Analysis and Simulation Modeling of Single-Event Transients in VLSI Circuits	Sect. 1.2
ECS	Embedded Computing systems	Sect. 2.1
FATAL	FWF P21994: A Modeling Framework for Fault-Tolerant Asynchronous Logic	Sect. 1.2.1
ODE	Ordinary differential equation	Sect. 1.3.2
RiSE/SHiNE	FWF S11405: Rigorous Systems Engineering	Sect. 1.2.1
SIC	FWF P26436: Self-stabilizing Byzantine Fault-Tolerant Distributed Algorithms for Integrated Circuits	Sect. 1.1
SPF	Short-Pulse Filtration Problem	Sect. 1.1
VLSI	Very-Large Scale Integration	Sect. 1.1

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