41st EOS/ESD Symposium and Exhibits

September 15 - 20, 2019

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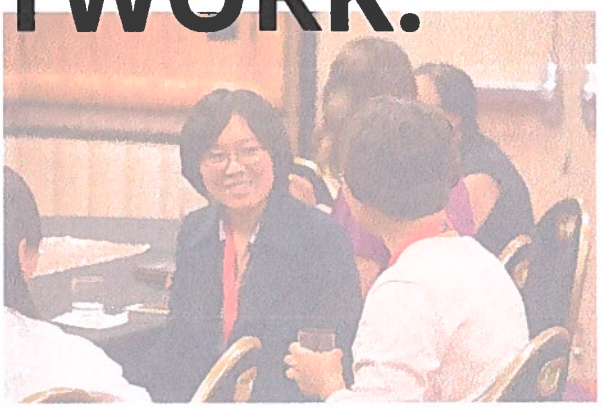

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Technical Sessions: Tuesday, September 17, Parallel Sessions

Exhibitor Showcase: 1:25 PM-1:35 PM

Transforming Technologies Booth 409

Session 2A: 1:35 PM-2:50 PM

2A: EOS/ESD Failure Analysis, Troubleshooting, and Case Studies I

Moderator: Ann Concannon, Texas Instruments, Inc.

2A.1 HV Latch-up at System Level ESD Current Injection
David Marreiro, Vladislav Vashchenko, Maxim Integrated Corp.

A correlation between JEDEC standard qualification HV latch-up test and a phenomenon of a similar nature induced by injection from system-level ESD pulse current is studied through comparison and additional TLP pseudo latch-up regimes. The initial insight about required layout spacing rules to withstand the ESD pulse injection HV latch-up conditions is presented.

2A.2 Mechanism of Sequential Finger Triggering of Multi-Finger Floating-Base SCRs Due to Inherent Substrate Currents
Hasan Karaca, Clément Fleury, Dionyz Pogany, TU Wien; Steffen Holland, Hans-Martin Ritter, Guido Notermans, Nexperia Germany GmbH

Sequential finger triggering (SFT) associated with successive voltage drops near the holding voltage is observed in multi-finger floating-base SCRs on SOI. The SFT is observed only for long pulse rise times (10 ns). TCAD simulation explains that 3-150 ns time delay between finger triggering is due to lateral carrier diffusion-limited processes.

2A.3 Dual Injection Latch-up Phenomenon in HV Rail Based ESD Protection Networks
Slavica Malobabic, David Marreiro, Vladislav Vashchenko, Maxim Integrated Corp.

A dual injection latch-up phenomenon in rail based ESD protection network was studied using wafer level experiments. When floating the ESD rail, low side injection causes positive feedback with high side diode connected to the power supply. Comparison of dual-injection latch-up vs. conventional HV low side latch-up isolation is presented.

Exhibitor Showcase: 1:25 PM-1:35 PM

Magwel NV Booth 110

Session 2B: 1:35 PM-2:50 PM

2B: Full-Custom and Application Driven ESD Concepts

Moderator: Christian Russ, Infineon Technology

2B.1 ESD Protection for Poly Fuses
Shao-Chang Huang, Li-Fan Chen, Chun-Chih Chen, Ting-You Lin, Kai-Chieh Hsu, Yeh-Ning Jou, Chih-Hsuan Lin, Yung-Chang Chen, Wei-Sung Chen, Jian-Hsing Lee, Vanguard International Semiconductor Corporation

Electrostatic discharge (ESD) can falsely program or erase the poly fuse cell even it has an ESD protection device. In this study, the phase change disabling circuit is successfully proposed and demonstrated that it can prevent the poly fuse from ESD damaging.

2B.2 Concurrent ESD and Surge Protection Clamps in RF Power Amplifier
Myunghwan Park, Jermyn Tseng, Tzung-yin Lee, David Ripley, Skyworks Solutions, Inc.

For cost reduction and device miniaturization efforts, the system-level surge suppressor is often being removed, which motivates developing concurrent HBM and surge protection clamps. Here, we characterize surge and HBM performance of the conventional clamps, and further propose a partial feedback combo clamp and ballasted RC-triggered clamp.

2B.3 A 3-Terminal HV-ESD Protection as Specialized Solution for EDn-MOSTs that Directly Link Two External Pads
Gijs de Raad, Da-Wei Lai, NXP Semiconductors

This paper describes ESD design around EDn-MOST devices that connect directly between two I/O pads. That ESD design involves carefully balancing the EDn-MOST drain voltage against its internal current density during ESD. A novel ESD device, the 3-port PNP, relaxes that balance and so increases design freedom.

Mechanism of Sequential Finger Triggering of Multi-Finger Floating-Base SCRs due to Inherent Substrate Currents

Hasan Karaca (1), Clément Fleury (1,2), Steffen Holland (3), Hans-Martin Ritter (3), Guido Notermans (3), Dionyz Pogany (1)

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(3) Nexperia Germany GmbH, Stresemannallee 101, 22529 Hamburg, Germany

Abstract - Successive voltage drops near the holding voltage associated with sequential finger triggering (SFT) are observed in multi-finger floating-base SCRs. A time delay between the triggering of neighboring fingers is in the 3-150ns range and it is observed only for long pulse rise times (10ns). TCAD simulation explains that SFT is due to lateral carrier diffusion-limited processes.

I. Introduction

Simultaneous triggering of multi-finger ESD protection devices is a long-standing goal of ESD engineers to improve ESD robustness [1-5]. Usually, for long pulse rise times (≥10ns), as in Human Body Model pulses [6], only a few fingers trigger and the next fingers trigger when the device voltage reaches the trigger voltage V_{TR} again, leading to a zigzag IV characteristics [3]. Short rise times help simultaneous triggering due to e.g. dV/dt effect [1]. Active schemes, such as substrate or gate coupling, have been proposed to trigger devices simultaneously or subsequently [3-5].

For system level protection, large multi-finger devices are often required to achieve robustness of the order of 30kV. SCR devices are suitable since they have low capacitance, low holding voltage and high failure current I_{t2} [7-8]. The high ESD robustness of these devices requires simultaneous or sufficiently fast triggering of device fingers.

In this work, we present an investigation of sequential finger triggering (SFT) observed in multi-finger floating-base SCRs of discrete technology [8]. The SFT is analyzed by Transient Interferometric Mapping (TIM) technique [9] and is observed only for long pulse rise time (10ns), where triggering of neighboring inner fingers occurs with a delay in the range of 3-150 ns, depending on the local current density. The SFT is associated with successive voltage drops near the holding voltage. Using TCAD, SFT is found to be a purely electrical effect limited only by the speed of the lateral carrier diffusion. Since there is no impact ionization at the triggering of inner fingers (i.e. the device voltage is much less than V_{TR}), the mechanisms of SFT is reminiscent of external latch-up of SCRs due to substrate currents [10].

The paper is organized as follows: Section II introduces devices and experimental methods, section III the experimental results. Section IV presents the simulation approach and section V the simulation results together with the explanation of the SFT mechanism followed by conclusions in section VI.

II. Devices and Experimental Methods

16-finger floating-base SCR devices with single finger width of W=25μm and finger pitch of ~11μm fabricated on lightly p-doped silicon-on-insulator (SOI) substrate [7] were studied (Fig. 1a). Fig.1b represents zoomed image for four fingers. The thickness of the active silicon layer is 1.5 um. n+-emitters (GND) of the npn transistor are grounded. The p+-emitters and n-wells are connected together and stressed positively. The n-well serves as a base and base resistance of the pnp transistor. A deep p-well, serving both as *base* of npn and collector of pnp is left *floating*, as is the substrate. In between the fingers there is no shallow trench isolation (STI) so all the active areas are connected through the same p-substrate, see Fig.1. The active fingers are labeled by '1' to '16' or