Digital Asynchronous Phase Locked Loop for Precision Control of MOEMS Scanning Mirror ⋆

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Abstract: Accurate phase detection and control of nonlinear resonant MOEMS mirrors are crucial to achieve stable scanning motions and high resolution imaging as needed in precision applications such as lidar systems. This paper proposes a novel digital PLL that uses an asynchronous logic for high precision driving of the MOEMS mirror and immediate phase compensation, while the clock speed is kept low. The phase of the mirror is detected by an amplified current signal, generated by the movement of the comb-drive electrodes and a simple comparator circuit. An analysis of the proposed detection method shows that the optical standard deviation of the system scales inversely proportional with the product of the driving voltage, the curvature of the comb-drive capacitance and the angular velocity of the MOEMS mirror at the zero crossing. The low phase detection standard deviation of 2.94 ns, in closed loop operation corresponds to a maximum optical standard deviation of 1 mdeg at 55.6° field of view and a scanning frequency of 2 kHz.

Keywords: Digital asynchronous phase locked loop (DAsPLL), Micro-Opto-Electro-Mechanical System (MOEMS), Resonant scanning mirror, Comb-drive, Nonlinear systems.

1. INTRODUCTION

Resonant micro-opto-electro-mechanical system (MOEMS) mirrors receive much attention in high precision scanning systems since they are cheap and easy to manufacture at small form factors and show high performance, as well as low power consumption (Petersen (1982)). A principle illustration of a 1D comb-drive actuated resonant MOEMS mirror is shown in Fig. 1, which are typically nonlinear oscillators. In order to achieve a large scan angle with a single MOEMS mirror they are often operated in the nonlinear regime and show high Q-factors even at atmospheric pressure. Additionally, actuators such as the electrostatic comb-drives show nonlinear voltage and position dependency, which makes the analysis of the mirror behavior more difficult (Sun et al. (2002); Pengwang et al. (2016)).

In high precision scanning imaging systems, accurate pixel synchronization to the mirror motion is critical for the image quality. For a targeted angular resolution of the system, the maximum angular velocity defines the required accuracy of the pixel triggering signals. Therefore the allowed pixel synchronization jitter scales inversely proportional with the mirror frequency as shown by Scholles et al. (2008) for a projection system. For example to achieve a SVGA resolution (800×600) with 50 frames per second, a fast axis scanning frequency of 47.1 kHz is needed, leading to a pixel duration of only 8.4 ns at the center.

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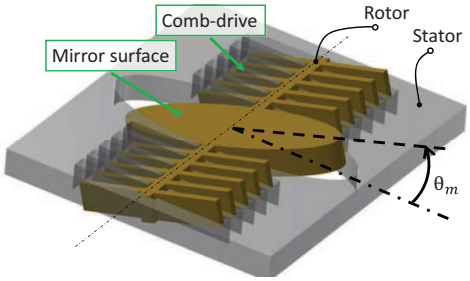

Fig. 1. Principle sketch of a general comb-drive actuated resonant scanning MOEMS mirror. Due to the symmetry of the electrostatic forces, the rotor is pulled to zero angle position, i.e. $\theta_m = 0°$, if a voltage is applied between the rotor and the stator electrodes.

In order to maintain the scanning trajectory even if environmental conditions change, a phase locked loop (PLL) is usually applied (Tortschanoff et al. (2010)). Various sensing methods for MOEMS mirror phase detection are proposed in literature, such as piezoresistive, piezoelectric, capacitive and optical. Piezoresistive and piezoelectric sensing methods are reported by Grahmann et al. (2011) and Baran et al. (2012), respectively, and can provide continuous angle measurement. These methods are subject of extensive research (e.g. Gu-Stoppel et al. (2017)), but suffer from durability and degradation problems. Furthermore the phase detection capability is not properly analyzed yet.

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The capacitive sensing methods are common for MOEMS mirrors (Chemmanda et al. (2014) and Cagdaser et al. (2004)), which use amplitude or frequency modulation of a high frequency carrier to extract the amplitude and phase information from the comb-drive capacitance variation. These capacitive methods, however, suffer from feedthrough of the driving signal to the sensing circuitry and are rather complicated. Roscher et al. (2003) proposed an alternative method using an external capacitor that integrates the current generated by the mirror movement. There is also an approach with dedicated comb-drives only for sensing, as proposed by Hofmann et al. (2012), which adds complexity to the design and therefore cost. However since the comb-drive capacitance is maximum at the zero crossing, all these capacitive methods have to resolve a peak transition in time, which is highly affected by measurement noise. Therefore usually low loop gains of the PLL are necessary to reduce the pixel synchronization jitter, which makes the PLL slow and may lead to instability if the mirror is disturbed by external influences.
The optical detection method proposed by Tortschanoff et al. (2010) uses photo diodes on the backside of the mirror and shows the lowest MOEMS mirror phase detection jitter reported in the literature so far, with a standard deviation of 12 ns for a mirror frequency of 23 kHz. However the design is more complex since additional optical components are required close to the MOEMS mirror.

The precision of the MOEMS mirror driving and pixel synchronization signals depend on both the phase detection capabilities as well as the PLL implementation. While analog PLLs (Li et al. (2012)) usually achieve high timing resolution, they consist of rather complicated circuitry and hardly allow complex control algorithms. On the other hand, digital PLLs (Roscher et al. (2003); Tortschanoff et al. (2010)) are easy to implement and provide many possibilities in control design, but require high clock speeds to resolve timing signals with high resolution.

The contribution of this paper is a digital asynchronous PLL (DAsPLL) with fast and high precision phase tracking capabilities based on a current measurement, without any additional component at the MOEMS mirror and simple circuitry. The mirror phase detector uses the amplified current signal generated by the movement of the comb-drive electrodes, which shows a sharp zero crossing when the mirror passes the maximum capacitance point, i.e. the zero angle position. The DAsPLL measures the mirror frequency and immediately compensates the phase difference by asynchronous switching of the driving voltage using the phase detector signals.

The paper is organized as follows. Section 2 describes the mirror phase detection method and the corresponding optical pointing uncertainty is discussed. Furthermore the DAsPLL principle and implementation is described. Section 3 provides the experimental results obtained in closed loop operation and in Section 4 the proposed DAsPLL is concluded.

2. MOEMS MIRROR CONTROL DESIGN

Figure. 2 shows a frequency response of the used comb-drive actuated resonant MOEMS mirror measured with a position sensitive detector (PSD) (Yoo et al. (2018)).

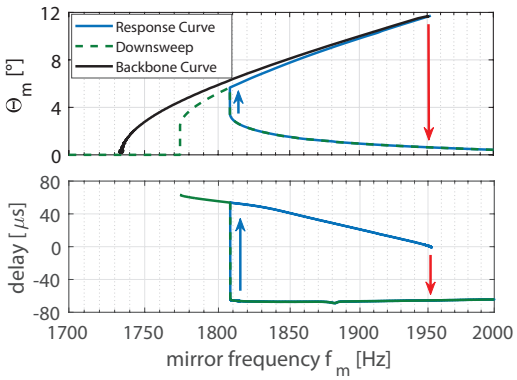

Fig. 2. Measured open loop frequency response of the used MOEMS mirror at 60 V square wave actuation. The blue arrow indicates a bifurcation point where an amplitude jump occurs. The amplitude further increases with increasing frequency until the fallback indicated by a red arrow.

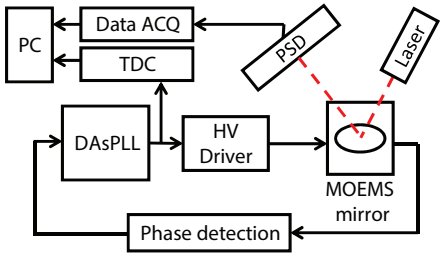

Fig. 3. Schematic of the measurement setup and the feedback loop for synchronized mirror operation with the DAsPLL. The mirror trajectory is measured by a PSD and a TDC provides a high resolution measurement of the digital driving signal period.

The driving voltage is a square wave signal (60 V, 50% duty cycle) whose frequency is twice the mirror frequency due to the characteristics of the comb-drive actuation. At increasing amplitudes the resonance frequency of the mirror also increases, which is called hardening behavior, and is also shown in the backbone curve obtained by a decay measurement. The delay provides the time difference between the negative edge of the driving voltage and the zero crossing of the mirror, i.e. the driving voltage is switched off after the zero crossing of the mirror if the delay is positive.

To drive the MOEMS mirror with maximum energy injection for a given voltage, synchronized excitation is proposed by Schenk et al. (2000). At synchronized excitation, the voltage is switched on when the mirror angle is at its maximum and switched off at the zero crossing, which corresponds to the zero delay condition in Figure. 2, i.e. highest amplitude point. However the synchronized excitation is an operation point at the boundary to the fallback, where the amplitude drops rapidly, and can be hardly achieved in open loop.

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Figure. 3 shows a simple schematic diagram of the measurement setup and the feedback loop. The MOEMS mirror trajectory is measured using a PSD while a time to digital converter (TDC) provides a precise measurement of the digital driving signal period.

The key elements of the feedback loop are the phase detector and the implemented PLL, which define the overall system performance. This section describes the developed phase detection method and provides an analysis of its timing jitter dependencies. Furthermore the working principle of the proposed DAsPLL is discussed.

2.1 Mirror Phase Detection

Accurate phase detection is necessary to keep the pixel synchronization jitter low in a PLL with a high loop gain, enabling fast tracking and precise driving of the MOEMS mirror. Therefore a highly sensitive phase detection method based on the current through the comb-drives is shown and analyzed in the following.

The capacitance between the rotor and stator comb-drive electrodes can be generally expressed as

$$C(\theta_m) = C_0 + C_\Delta(\theta_m)\,, \tag{1}$$

where θ_m is the mechanical mirror angle, C_0 is the comb-drive capacitance at zero angle and $C_\Delta(\theta_m)$ is the variable capacitance with $C_\Delta(0) = 0\,\mathrm{F}$.

Besides the transient behavior at the edges of the square wave driving signal, the applied voltage between the comb-drive electrodes is constant, and the measured current can be expressed as

$$I = V\,\frac{dC(\theta_m)}{dt} = V\,\frac{dC_\Delta(\theta_m)}{d\theta_m}\,\frac{d\theta_m}{dt}\,, \tag{2}$$

where $\frac{dC_\Delta(\theta_m)}{d\theta_m}$ is a pure geometrical parameter. The variable comb-drive capacitance and its angular derivative are shown in Fig. 4 which are obtained by an actuated decay measurement (Brunner et al. (2019)). It shows that the current provides a zero crossing when the mirror crosses the position with maximum capacitance, i.e. the zero angle position. Using this property, the simplest implementation of a phase detector is a comparator with a threshold corresponding to zero current, that provides a digital signal to the DAsPLL.

The phase detection jitter is then defined by the steepness of the current at the zero crossing, which can be calculated to

$$\frac{dI}{dt} = V\left[\frac{d^2C_\Delta(\theta_m)}{d\theta_m^2}\left(\frac{d\theta_m}{dt}\right)^2 + \frac{dC_\Delta(\theta_m)}{d\theta_m}\,\frac{d^2\theta_m}{dt^2}\right], \tag{3}$$

where the second term in the square brackets is negligible at $\theta_m = 0°$, since the capacitance gradient and the inertial forces are low. Therefore the steepness of the current generated by the comb-drive electrodes at the zero crossing scales with the nonzero product of the applied voltage, the curvature of the comb-drive capacitance and the squared mirror angular velocity.

Assuming a constant additive Gaussian noise with the standard deviation σ_I on the current signal, the standard deviation of the phase detection can be expressed as

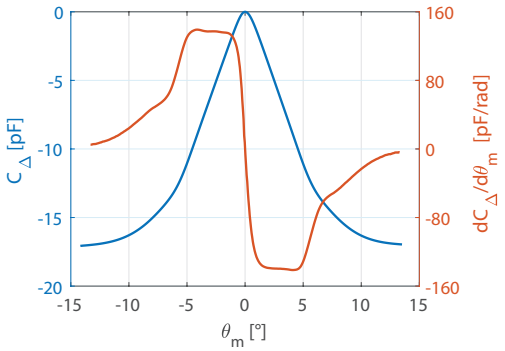

Fig. 4. Measured comb-drive capacitance and its angular derivative of the MOEMS mirror, estimated by an actuated decay measurement. Since the capacitance is maximum at zero angle of the mirror, its derivative provides a sharp zero crossing.

$$\sigma_{\Delta t} = \left.\frac{dt}{dI}\right|_{\theta_m=0°}\sigma_I = \left(V\left.\frac{d^2C_\Delta(\theta_m)}{d\theta_m^2}\right|_{\theta_m=0°}\dot{\Theta}_m^2\right)^{-1}\sigma_I\,, \tag{4}$$

where $\dot{\Theta}_m$ is the amplitude of the mirror angular velocity. The accuracy of the phase detection is therefore disproportionately increasing for faster mirrors. However faster mirrors also demand a better pixel synchronization for the same optical standard deviation. If the laser is shot directly with the phase detection signal, the optical standard deviation at the zero crossing of the mirror is given by $\sigma_{opt} = 2\,\dot{\Theta}_m\,\sigma_{\Delta t}$. With (4), σ_{opt} can be expressed as

$$\sigma_{opt} = 2\left(V\left.\frac{d^2C_\Delta(\theta_m)}{d\theta_m^2}\right|_{\theta_m=0°}\dot{\Theta}_m\right)^{-1}\sigma_I\,. \tag{5}$$

Equation (5) shows how the minimum pixel size of the scanning system depends on the MOEMS design parameters and operation condition when the phase signal directly triggers the laser shot. It shows that the system performance can be increased by increasing the driving voltage, the curvature of the comb-drive capacitance or the mirror angular velocity. However as given in (3), the bandwidth of the current sensing amplifier may also have to be increased, leading to an increase of the sensing noise.

2.2 Digital Asynchronous PLL

The injected comb-drive energy per actuation period can be expressed as

$$E_{comb} = \frac{1}{2}\,V^2\left[C_\Delta\big(\theta_m(t_{off})\big) - C_\Delta\big(\theta_m(t_{on})\big)\right], \tag{6}$$

where transients are neglected and t_{off} and t_{on} are the switching off and on time of the square wave driving signal, respectively (See Brunner et al. (2019)). Therefore the injected energy is only defined by these two time instances and the influence of driving jitter can be analyzed by the local time derivatives. Using a taylor approximation of up to the second order, the injected energy change can be expressed as

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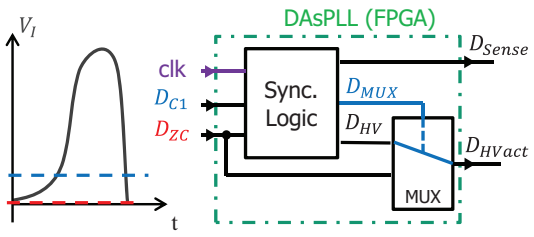

Fig. 5. Operation principle of the DAsPLL. (left) Illustration of a current signal V_I with comparator threshold values given by dashed lines. (right) DAsPLL scheme, consisting of a synchronized logic and an asynchronous multiplexer (MUX). The multiplexer is controlled by the synchronized logic and connects the driving output D_{HVact} directly to the zero crossing comparator signal D_{ZC} if a negative edge is detected on D_{C1}. Also a current sensing enable signal D_{Sense} is provided for high switching transient suppression.

$$\begin{aligned}\Delta E_{comb} \approx \frac{1}{2} V^2 \Bigg[& \frac{dC_\Delta\left(\theta_m\left(t_{off}\right)\right)}{dt} \Delta t_{off} \\ & + \frac{1}{2} \frac{d^2 C_\Delta\left(\theta_m\left(t_{off}\right)\right)}{dt^2} \Delta t_{off}^2 \\ & - \frac{dC_\Delta\left(\theta_m\left(t_{on}\right)\right)}{dt} \Delta t_{on} \\ & - \frac{1}{2} \frac{d^2 C_\Delta\left(\theta_m\left(t_{on}\right)\right)}{dt^2} \Delta t_{on}^2 \Bigg],\end{aligned} \tag{7}$$

where Δt_{off} and Δt_{on} are the corresponding timing jitter. Using (2), (7) can be rewritten to

$$\begin{aligned}\Delta E_{comb} \approx \frac{1}{2} V \Bigg[& I(t_{off}) \Delta t_{off} + \frac{1}{2} \frac{dI(t_{off})}{dt} \Delta t_{off}^2 \\ & - I(t_{on}) \Delta t_{on} - \frac{1}{2} \frac{dI(t_{on})}{dt} \Delta t_{on}^2 \Bigg].\end{aligned} \tag{8}$$

Equation (8) shows the benefit of synchronized excitation, since both $I(t_{off})$ and $I(t_{on})$ are zero at the switching points, leading to a low disturbance of the mirror motion by the driving jitter. However the driving voltage should be accurately switched off at the zero crossing due to the high current gradient, while the switching on time is more relaxed especially if the mirror is at a high amplitude. Therefore a DAsPLL is developed that switches the driving voltage with the phase detection signal asynchronously to the internal clock, while the switching on time is provided by a synchronized logic.

The principle implementation of the DAsPLL is shown in Fig. 5. Two comparator signals are the inputs to the DAsPLL, which have negative edges successively in time at a zero crossing of the mirror. The synchronized logic block calculates the mirror period from adjacent zero crossings of the mirror, using the comparator signals and provides a current sensing enable signal D_{Sense}, a driving signal D_{HV} and a multiplexer control signal D_{MUX}. D_{Sense} is used for safe operation of the current sensing circuitry and is discussed in the following section. At a detected zero crossing, a counter is triggered that holds D_{HV} low for a quarter mirror period until it gets high again, waiting for the next zero crossing of the mirror. Therefore a square wave signal is generated which is governed by the mirror movement.

In order to accurately switch the voltage off at the zero crossing of the mirror without clock dependency, an asynchronous multiplexer MUX is implemented. The negative edge of the first comparator is used to switch the asynchronous multiplexer such that it connects the zero crossing comparator signal directly to the driving output D_{HVact} of the DAsPLL. Therefore when the current hits the zero crossing comparator threshold, the signal is forwarded to the driving circuitry and switches the voltage at the mirror off. After at least one clock cycle the multiplexer is switched back again and connects the synchronized driving signal D_{HV} to the driving output.

The threshold of the first comparator has to be properly chosen and depends on the obtained current signal, measurement noise and the internal clock of the DAsPLL. The higher the threshold, the higher the required current signal, since it has to cross the threshold. A too low threshold however may increase the risk of false detections due to sensing noise, which may result in malfunctioning. Furthermore the time between the crossing of the first comparator and the zero crossing comparator has to be at least one clock cycle.

The DAsPLL immediately compensates the phase error with high accuracy and stabilizes the MOEMS mirror even though it has nonlinear dynamics. Since the measured mirror frequency only defines the time when the driving signal is switched on again after a zero crossing, it can be internally averaged to reduce measurement errors, without loss of track. The DAsPLL is therefore directly following the mirror motion, which is fundamentally different from conventional PLLs for nonlinear systems which usually only adapt their frequency regarding the measured phase error (Fan et al. (2007)).

3. EXPERIMENTAL RESULTS

Figure. 6 shows the used driving circuitry and a principle signaling example. The rotor potential of the mirror can be controlled by only one digital input D_{HVact}, i.e. generating square wave signals. A second digital input D_{Sense} enables the measurement of the current collected by the stator comb-drive electrodes via an instrumentation amplifier. The delayed turning on of D_{Sense} is to suppress the high transient current generated by the fast switching of the MOSFETs and to avoid damage of the instrumentation amplifier.

The DAsPLL is implemented in FPGA (Zedboard, Avnet, Phoenix, US) and operated at 50 MHz internal clock. Fig. 7 shows the measured signals in closed loop operation. The driving signal is accurately switched off at the zero crossing of the mirror trajectory and switched on again after a quarter mirror period, establishing synchronized excitation. A TDC (GPX2, AMS, Premstaetten, AT) is used to measure the period variation of the DAsPLL with 20 ps resolution, where the period is defined by two adjacent negative edges of the digital driving signal. The TDC measures every other DAsPLL period, which corresponds

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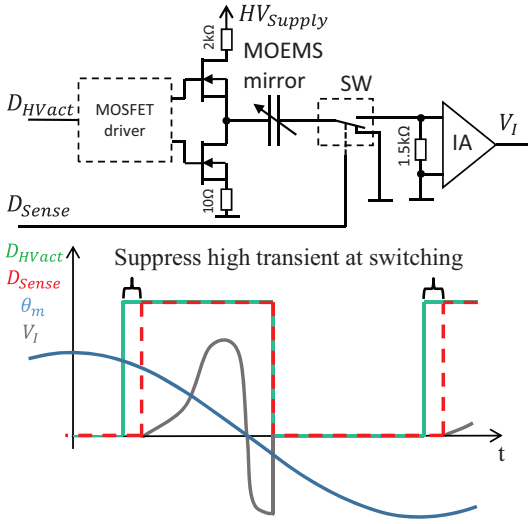

Fig. 6. (top) Used MOSFET half-bridge to drive the MOEMS mirror, which is electrically modeled as a variable capacitance, with square wave signals controlled by a single digital input D_{HVact}. The input D_{Sense} controls the analog switch (SW). The instrumentation amplifier (IA) provides an analog signal V_I which is proportional to the current through the MOEMS capacitance if D_{Sense} is high. (bottom) Principle signaling example for current sensing.

to either the positive or negative half period of the mirror. Figure 8 shows a histogram of the measured DAsPLL output frequency. Due to the asynchronous switching, a Gaussian shape is obtained without timing quantization. This originates from a white noise source given by the current sensing circuitry and therefore directly reflects the phase detection jitter.

Considering the working principle of the DAsPLL, the measured driving period can be expressed as

$$T_i = \Delta t_{i-1} + T_{m,i} - \Delta t_i \tag{9}$$

where Δt_i and $T_{m,i}$ are the phase detection error and the corresponding mirror half period at the i-th period, respectively. Assuming that the mirror period is hardly affected by the driving jitter at synchronized excitation, the phase detection error is uncorrelated and its standard deviation can be approximated by

$$\sigma_{\Delta t} \approx \frac{\sigma_T}{\sqrt{2}} \,. \tag{10}$$

The phase detection standard deviation $\sigma_{\Delta t}$ is therefore 2.94 ns at the used operation point ($\Theta_m = 13.91°$ and $f_m = 2022.472$ Hz), which corresponds to an optical standard deviation of only $\sigma_{opt} = 1.04$ mdeg.

As the DAsPLL locks on the mirror movement, the only remaining input to the system is the driving voltage, which defines the operation point of the MOEMS mirror in closed loop. Table 1 shows the reached mechanical amplitudes and frequencies for different driving voltages. Figure 9 shows the obtained phase detection standard

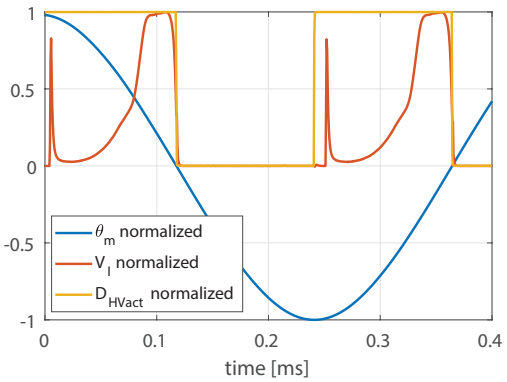

Fig. 7. Measured signals at closed loop operation (70 V). The negative edge of the digital driving signal D_{HVact} coincides with the zero crossing of the current and therefore with the zero crossing of the mirror trajectory θ_m. A quarter mirror period after the zero crossing the digital driving signal gets high again, establishing synchronized excitation of the MOEMS mirror. The sharp peaks in the current signal are a measurement artifact caused by the switching of the analog switch SW.

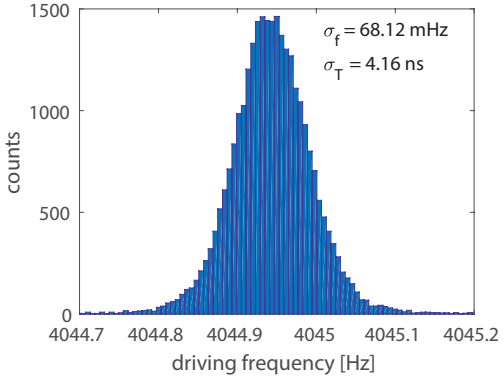

Fig. 8. Histogram of the digital driving signal frequency, defined by adjacent negative edges, in closed loop operation (70 V) measured by a TDC. The low standard deviations in frequency σ_f and period σ_T clearly show the superior performance of the proposed DAsPLL. Due to the asynchronous logic, the shape of the histogram is governed by white noise and is therefore Gaussian without showing quantization steps even though the clock cycle is 20 ns (50 MHz).

deviations compared to a theoretical model based on (4), by using the applied voltage and the mirror velocity amplitude measured by a PSD. The results show that the performance of the proposed DAsPLL with current sensing based phase detection scales with the mirror operation point as predicted by the theoretical model (4) and that a low phase detection standard deviation of 2.94 ns is achieved.

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Table 1. Measured mechanical amplitude and frequency of the MOEMS mirror at closed loop operation for different driving voltages.

HV_{Supply} [V]	Θ_m [°]	frequency f_m [Hz]
40	8.65	1870.307
50	10.57	1922.793
60	12.30	1973.742
70	13.91	2022.472

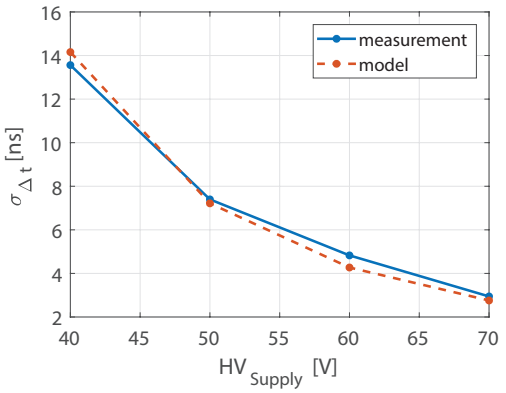

Fig. 9. Phase detection standard deviation in closed loop operation at different driving voltages HV_{Supply} measured by a TDC. A phase detection error model $\hat{\sigma}_{\Delta t} = \sigma_0 \left(V \dot{\Theta}_m^2\right)^{-1}$ is fitted, with $\dot{\Theta}_m$ measured by the PSD and a fitting constant σ_0.

4. CONCLUSION

A simple high precision driving and fast tracking DAsPLL for MOEMS mirrors is proposed, utilizing a current sensing based phase detection and asynchronous logic. The zero crossing of the mirror is measured by the current generated by the moving comb-drive electrodes, providing a high resolution phase detection with simple comparators. The DAsPLL is implemented in FPGA and consists of a synchronized logic and an asynchronous multiplexer, which accurately switches the driving signal according to the mirror movement. The phase error is immediately compensated in each period while the frequency of the DAsPLL can be averaged without loss of track. Experimental results show a phase detection jitter that corresponds to a maximum optical standard deviation of 1 mdeg at 55.6° field of view and a scanning frequency of 2 kHz. The provided scaling laws suggest that the proposed system can be a possible solution for high resolution scanning at frequencies of several tens of kilohertz.

REFERENCES

Baran, U., Brown, D., Holmstrom, S., Balma, D., Davis, W.O., Muralt, P., and Urey, H. (2012). Resonant pzt mems scanner for high-resolution displays. *Journal of Microelectromechanical Systems*, 21(6), 1303–1310.

Brunner, D., Yoo, H.W., Thurner, T., and Schitter, G. (2019). Data based modelling and identification of nonlinear sdof moems mirror. Proceedings Volume 10931, MOEMS and Miniaturized Systems XVIII.

Cagdaser, B., Jog, A., Last, M., Leibowitz, B.S., Zhou, L., Shelton, E., Pister, K.S.J., and Boser, B.E. (2004). Capacitive sense feedback control for mems beam steering mirrors.

Chemmanda, L.J., Jianrong, C.C., Singh, R.P., and Roterman, Y. (2014). Asic front-end for sensing mems-mirror position. In *2014 International Symposium on Integrated Circuits (ISIC)*, 396–399.

Fan, M., Clark, M., and Feng, Z. (2007). Implementation and stability study of phase-locked-loop nonlinear dynamic measurement systems. *Communications in Nonlinear Science and Numerical Simulation*, 12(7), 1302 – 1315.

Grahmann, J., Graßhoff, T., Conrad, H., Sandner, T., and Schenk, H. (2011). Integrated piezoresistive position detection for electrostatic driven micro scanning mirrors. volume 7930, 7930 – 7930 – 8.

Gu-Stoppel, S., Giese, T., Quenzer, H.J., Hofmann, U., and Benecke, W. (2017). Pzt-actuated and -sensed resonant micromirrors with large scan angles applying mechanical leverage amplification for biaxial scanning. *Micromachines*, 8(7).

Hofmann, U., Janes, J., and Quenzer, H.J. (2012). High-q mems resonators for laser beam scanning displays. *Micromachines*, 3(2), 509–528.

Li, H.C., Tseng, S.H., Huang, P.C., and S.-C. Lu, M. (2012). Study of cmos micromachined self-oscillating loop utilizing a phase-locked loop-driving circuit. *Journal of Micromechanics and Microengineering*, 22.

Pengwang, E., Rabenorosoa, K., Rakotondrabe, M., and Andreff, N. (2016). Scanning micromirror platform based on mems technology for medical application. *Micromachines*, 7(2).

Petersen, K.E. (1982). Silicon as a mechanical material. *Proceedings of the IEEE*, 70(5), 420–457.

Roscher, K.U., Fakesch, U., Schenk, H., Lakner, H.K., and Schlebusch, D. (2003). Driver asic for synchronized excitation of resonant micromirrors. volume 4985, 4985 – 4985 – 10.

Schenk, H., Durr, P., Haase, T., Kunze, D., Sobe, U., Lakner, H., and Kuck, H. (2000). Large deflection micromechanical scanning mirrors for linear scans and pattern generation. *IEEE Journal of Selected Topics in Quantum Electronics*, 6(5), 715–722.

Scholles, M., Bruer, A.H., Frommhagen, K., Gerwig, C., Lakner, H.K., Schenk, H., and Schwarzenberg, M. (2008). Ultracompact laser projection systems based on two-dimensional resonant microscanning mirrors. *Journal of Micro/Nanolithography, MEMS, and MOEMS*, 7, 7 – 7 – 11.

Sun, X., Horowitz, R., and Komvopoulos, K. (2002). Stability and resolution analysis of a phase-locked loop natural frequency tracking system for mems fatigue testing. *Journal of Dynamic Systems Measurement and Control-transactions of The Asme*, 124.

Tortschanoff, A., Lenzhofer, M., Frank, A., Wildenhain, M., Sandner, T., Schenk, H., Scherf, W., and Kenda, A. (2010). Position encoding and phase control of resonant moems mirrors. *Sensors and Actuators A Physical*, 162, 235–240.

Yoo, H.W., Druml, N., Brunner, D., Schwarzl, C., Thurner, T., Hennecke, M., and Schitter, G. (2018). Mems-based lidar for autonomous driving. *Elektrotechnik und Informationstechnik*, 135(6), 408–415.

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