10:30 Coffee Break

Session SS Special Session Space and Aeronautic systems

Room Cassiopée

chairpersons M. LABRUNEE
P. PONS

10:50 **SS-1 #17** *Stress factors in aircraft electronics: superimpositions, case studies and failure precautions*
P. Jacob, G. Nicoletti
Empa Swiss Fed Labs for Materials Testing and Research

11:10 **SS-2 #25** *A closed-loop voltage prognosis for lithium-ion batteries under dynamic loads using an improved equivalent circuit model*
J. Yang[1], J. Yu[1], D. Tang[1], J. Dai[2]
[1]Beihang University, [2]China Academy of Launch Vehicle Technology R&D Center

11:30 **SS-3 #84** *Combined Ionizing Radiation & Electromagnetic Interference Test Procedure to Achieve Reliable Integrated Circuits*
F. Vargas[1], R. Goerl[1], P. Villa[2], N. Medina[3], N. Added[3], M. Da Silva[4]
[1]Catholic University - PUCRS, [2]Federal Institute of Rio Grande do Sul - IFRS, [3]University of São Paulo, [4]Centro Universitário FEI

11:50 **SS-4 #127** *Robustness and Reliability Review of Si and SiC FET devices for More-Electric-Aircraft Applications*
J. Ortiz Gonzalez, R. Wu, S. N. Agbo, O. Alatise
The University of Warwick

12:10 **SS-5 #219** *Reliability evaluation of a 0.25µm SiGe technology for space applications*
C. Robin, S. Rochette
Thales Alenia Space

12:30 **SS-6 #241** *Radiation-induced Single Event Transient effects during the Reconfiguration Process of SRAM-based FPGAs*
L. Sterpone, C. De Sio, L. Bozzoli, S. Azimi, B. Du
Politecnico di Torino

12:50 Lunch

Session I1-I2 ESD and EMC

Room Cassiopée

chairpersons D. POGANY
T. DUBOIS

14:00 Invited paper
EMC & ESD from the technology to the system (Challenge, Trends, application cases)
P. Besse
NXP Semiconductors

14:40 **I1-I2-1 #37** *Effect of TLP rise time on ESD failure modes of collector-base junction of SiGe heterojunction bipolar transistors*
C. Fleury[1], D. Pogany[2], W. Simbürger[3]
[1]CTR Carinthian Tech Research AG, [2]Vienna University of Technology, [3]Infineon

15:00 **I1-I2-2 #39** *Topology and design investigation on thin film silicon BIMOS device for ESD protection in FD-SOI technology*
P. Galy[1], L. De Conti[2], M. Vinet[3], S. Cristoloveanu[4],