Microelectronics Reliability 100–101 (2019) 113482

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Stress and Recovery Dynamics of Drain Current in GaN HD-GITs Submitted to DC Semi-ON stress

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ABSTRACT

Stress and recovery dynamics of the drain current are analysed in normally-off GaN Hybrid-Drain - embedded Gate Injection Transistors (HD-GITs) submitted to a semi-ON state stress. Under this condition moderate drain current and high drain voltage (350-650 V) are applied simultaneously. During the stress phase the drain current shows a remarkable decrease due to hot carrier trapping and is dependent on the applied drain voltage, stress current and temperature (30–190 °C). This degradation is fully recoverable, either thermally in the temperature range 150–190 °C or by hole injection from the gate. We provide a model for the detrapping time constant taking into account both the thermally-driven process dominating for gate biases $V_{GS} < 3$ V and hole capture dominant for $V_{GS} > 3$ V.

1. Introduction

GaN HEMTs are promising devices for power applications thanks to the wide bandgap of GaN enabling high breakdown field and high current density [1].

Since normally-OFF operation is strongly desired, devices with p-doped gates have been introduced. One of those device types allows a strong injection of holes from the gate and therefore is called Gate Injection Transistor (GIT) [2].

One of the main issue of a GaN HEMT is the increase in the dynamic on-resistance and the current collapse, increasing the ON-state losses and decreasing the drain current after the application of high voltage [3]. Kaneko et al. proposed the Hybrid Drain-embedded GIT (HD-GIT) [4] where the drain terminal is electrically connected to a p-drain region in order to suppress the current collapse after OFF-state stress through the injection of holes from the p-drain [4,5]. Even if this solves the problem of dynamic on-resistance under OFF-state conditions, this effect is still present during semi-ON operations. The simultaneous presence of moderate current and high voltage can produce hot electrons causing further charge trapping that is not present during OFF-state operation [6,7]. The impact of hot electrons is influenced by various factors like the electric field, drain current density and temperature. It has been suggested that the recovery is accelerated by the neutralization of negatively charged defects by the capture of holes injected from the gate [9,10]. Fabris et al. [7] have additionally considered that the recovery is governed by a thermally-driven process.

In this study we present detailed analysis of the drain current dynamics during both the stress and recovery in HD-GITs subjected to DC semi-ON stress as well as their dependence on bias, current and temperature. Part 2 describes the devices, DC characterization and basic comparison of OFF-state and semi-ON stress. Part 3 introduces the performed transient measurements and analyses the influence of bias, current and temperature on the stress and recovery behavior. For the recovery we develop a model based on defect capture-emission kinetics that combines the thermal and hole capture – induced mechanisms and explains the experiments.

2. Devices and DC characterization

The analysed HD-GITs (Fig. 1) test structures have a gate width of 200 µm, a gate length of 1.2 µm and a gate drain distance of 10 µm. The devices, epitaxially grown on 6 inch Si(111) wafers, have a p-doped GaN gate with a recessed and regrown AlGaN barrier below the gate [4]. The GaN buffer is compensated by Carbon doping in the range of 10^{19} cm^{-3}.The threshold voltage V_{TH} at room temperature is 1.5 V. Fig. 2(a) and (b) show respective I_D-V_{GS} and I_G-V_{GS} characteristics with the temperature T as parameter for a virgin device.

A point with zero-temperature dependence occurs at $V_{GS} = 1.6$ V (Fig. 2(a)). For $V_{GS} < 1.6$ V the drain current increases with temperature due to decrease in V_{TH} with temperature, while for $V_{GS} > 1.6$ V the current decreases due to mobility degradation, similarly as e.g. in [11]. The ideality factor n of the I_G-V_{GS} characteristics varies from $n = 5$–6 at $V_{GS} = 2$–3 V to $n = 4$–5 at $V_{GS} = 3$–4 V.

Fig. 3(a, b) present the comparison of DC *I-V* characteristics before

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https://doi.org/10.1016/j.microrel.2019.113482
Received 15 May 2019; Received in revised form 14 June 2019; Accepted 31 July 2019
Available online 23 September 2019

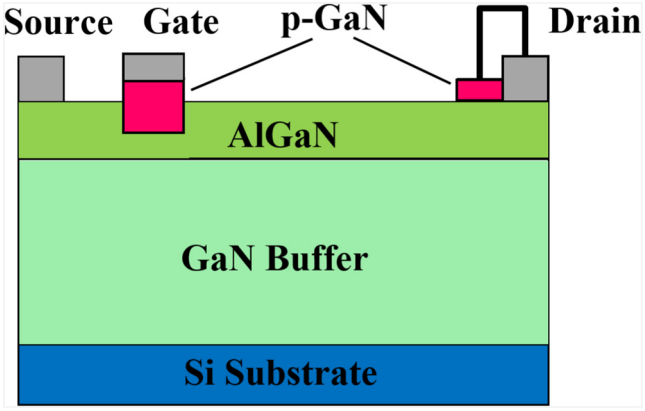

Fig. 1. Schematic cross section of a Hybrid Drain-emebedded Gate Injection Transistor (HD-GIT).

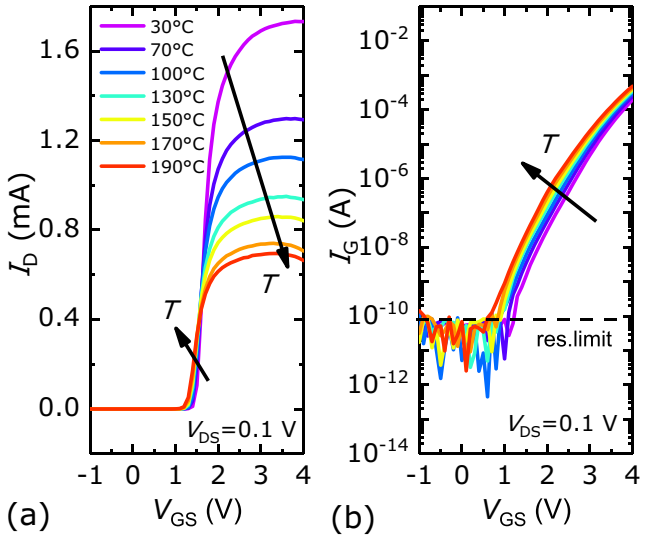

Fig. 2. (a) I_D-V_{GS} and (b) I_G-V_{GS} characteristics at V_{DS} = 0.1 V at different temperatures.

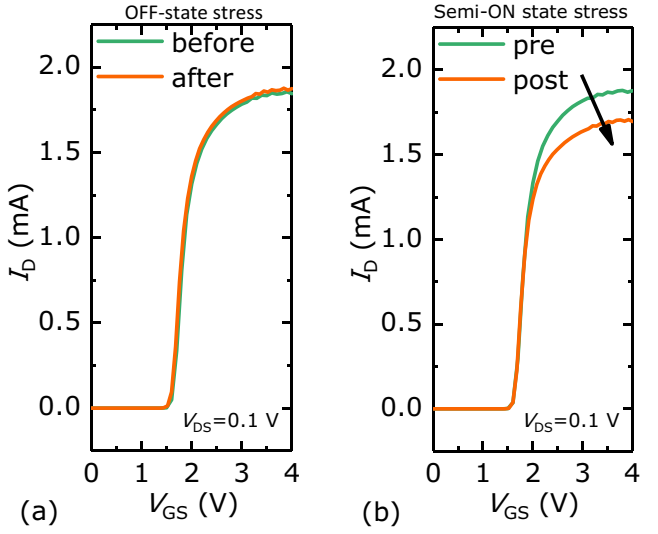

Fig. 3. Room temperature I_D-V_{GS} characteristics before and after stress of the device subjected to (a) OFF-state and (b) semi-ON stress.

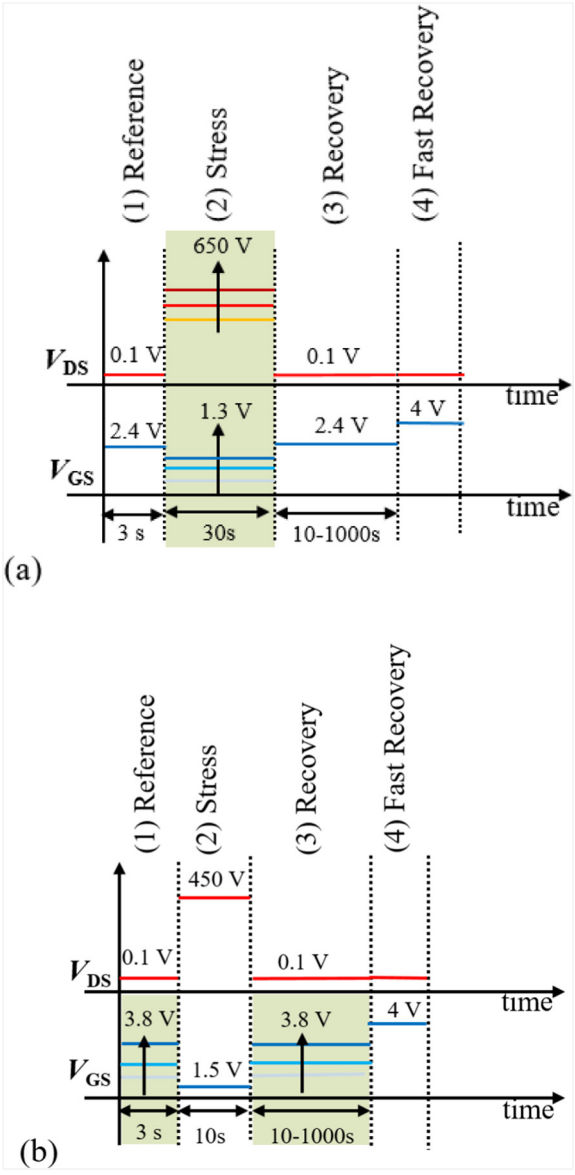

Fig. 4. Measurement sequence consisting of reference, stress and recovery phases. (a) For stress analysis the drain voltage $V_{DS,str}$ and the gate voltage $V_{GS,str}$ during stress are varied, while (b) for recovery analysis $V_{GS,rec}$ during the recovery and reference phases is varied. The temperature in all phases is the same.

and after the OFF-state stress (drain voltage $V_{DS,str}$ = 450 V, gate voltage $V_{GS,str}$ = 0 V for 10 s) and semi-ON state stress ($V_{DS,str}$ = 450 V, $V_{GS,str}$ = 1.5 V for 10 s), respectively. The averaged current during the OFF-stress is nearly 0.3 nA, while the current during the ON-stress is about 0.5 mA (see next section).

While the device subjected to OFF-state stress does not exhibit any stress-induced change in I_D-V_{GS} characteristics (Fig. 3(a)), the current after the semi-ON stress decreases (Fig. 3(b)) which is ascribed to hot carrier trapping in the GaN buffer [6,7]. We can exclude that the decrease in Fig. 3(b) is due to significant self-heating as we take care that the power dissipated is below 500 mW. We also notice that the hysteresis in the measured I_D-V_{GS} characteristics for the voltage sweeping rate of 4 V/s is < 50 mV.

3. Transient measurements in semi-ON stress

3.1. Stress-recovery sequence and transients

In all experiments the chip's back side (i.e. substrate) is connected to the source. Since the drain current degradation after the stress is fully recoverable at high gate currents the same device can be used repeatedly with varying stress and recovery parameters. Fig. 4(a, b) show one cycle of the measurement sequence used in respective stress and recovery experiments where the drain current transients during the stress and recovery phases are monitored.

They are composed of four different phases:

(1) reference measurement where the initial drain current $I_{D,0}$ is measured for 3 s serving as reference before stress;
(2) transient I_D measurement during stress for the duration t_{str};
(3) transient I_D measurement during recovery for the duration t_{rec}, which is chosen sufficiently long in order to extract a time constant, i.e. 10–1000 s;
(4) fast recovery at high gate current which resets the device back to its initial state (V_{GS} = 4 V is sufficient to fully recover the device in about 1 s).

In the stress experiments (Fig. 4(a)) $V_{DS,str}$ and $V_{GS,str}$ in the stress phase (2) are sequentially increased ($V_{DS,str}$ from 350 to 650 V; $V_{GS,str}$ from 0.7 to 1.3 V) for t_{str} = 30 s while the recovery parameters are fixed. In this way it is possible to analyse the impact of the $V_{DS,str}$ and the drain current $I_{D,str}$ (i.e. varied $V_{GS,str}$).

In the recovery experiments (Fig. 4(b)), the stress parameters $V_{DS,str}$ and $V_{GS,str}$ are fixed for t_{str} = 10 s, while $V_{GS,rec}$ in each cycle varies simultaneously with V_{GS} in the reference measurements to have adequate reference for the drain current degradation for varying $V_{GS,str}$. For reason of comparison all the measurements are performed with $V_{DS,rec}$ = 0.1 V, i.e. in the linear regime.

Typical drain current evolution during the stress ($V_{DS,str}$ = 450 V;$V_{GS,str}$ = 1.5 V) for three different temperatures are given in Fig. 5(a). The current typically decreases, even if some increase for a short time is observed at room temperature. Typical recovery transients for three different temperatures are given in Fig. 5(b). The transients are close to exponential.

In Fig. 5(b) the current transients I_D(t) are normalized to their corresponding initial values $I_{D,0}$, obtained in the reference period. We define as degradation parameter D:

$$D = 1 - \frac{I_D(t_{rec} = 100\ \text{ms})}{I_{D,0}}, \quad (1)$$

It is important to point out that this kind of severe stress we use in our experiments is not present under typical operation conditions. In a real switching application the device crosses three consecutive regimes: OFF-state (high voltage), semi-ON-state (high current and high voltage) and ON-state (high current). In our experiments we use stress conditions of the order of seconds, while in the real applications it is only a fraction of this. Additionally, the following ON-state period with the gate voltage above V_{TH} in application allows hole injection and hence a full recovery of trapped charges during a switching cycle.

3.2. Stress analysis

In this subsection the degradation will be studied as a function of different stress conditions. Fig. 4(a) shows that in our experiments $V_{GS,str}$ is varied from 0.7 V to 1.3 V. Since we are interested in the effect of stress current (i.e. the amount of injected hot electrons) we will use the $I_{D,str}$ as parameter.

In order to have a well measurable degradation we chose a stress time t_{str} of 30 s. The graph in Fig. 5(a) shows that the $I_{D,str}$ decreases with time, while the degradation D increases with time (not shown). So in order to get the maximum degradation we select the value at the end

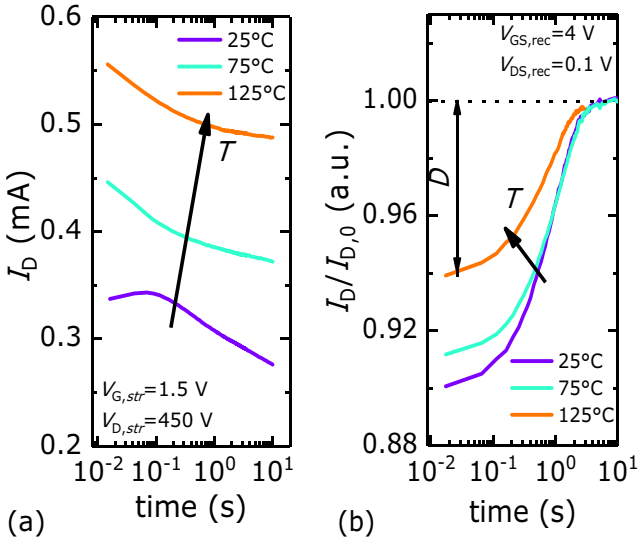

Fig. 5. Examples of drain current transients during (a) stress and (b) recovery for three different temperatures. V_{GS} and V_{DS} during stress and recovery phase are indicated in the figures. The degradation parameter D for 125 °C is indicated in (b).

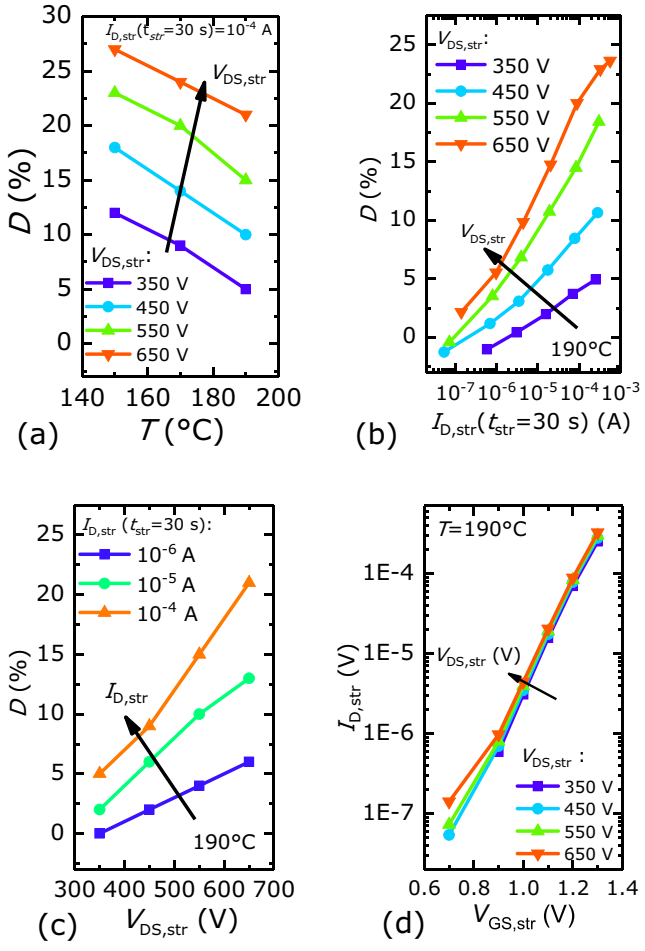

Fig. 6. Degradation parameter D as a function of the (a) temperature T for different $V_{DS,str}$ at $I_{D,str}$ = 10^{-4} A; (b) stress current $I_{D,str}$ at t_{str} = 30 s for different $V_{DS,str}$ at T = 190 °C; (c) $V_{DS,str}$ for different $I_{D,str}$ a T = 190 °C. (d) $I_{D,str}$ (t_{str} = 30 s) as a function of the $V_{GS,str}$ for different $V_{DS,str}$ at T = 190 °C.

of the stress, i.e. $I_{D,str}$ at t_{str} = 30 s ($I_{D,str}(t_{str}$ = 30 s)).

Fig. 6(a) shows D as a function of the temperature with $V_{DS,str}$ as parameter. These results highlight that for the same stress current D decreases with T, which can have two origins: 1) At higher temperature phonon scattering increases so that a smaller number of high-energetic carriers is available for trapping, thus decreasing D. 2) It is also possible that during the stress phase, parallel to trapping significant thermal detrapping occurs, shifting the total amount of trapped charges to lower values.

Fig. 6(b) and (c) report, respectively, the degradation parameter D at T = 190 °C as a function of the stress current $I_{D,str}(t_{str}$ = 30 s) for different $V_{DS,str}$ and as a function of $V_{DS,str}$ for different $I_{D,str}(t_{str}$ = 30 s). For clarity we also show in Fig. 6(d) the dependence of $I_{D,str}$ at T = 190 °C on control variable $V_{GS,str}$ for different $V_{DS,str}$. This sub-threshold IV characteristics show that the dependence is exponential and almost independent on $V_{DS,str}$.

The Figs. 6(b, c) show that D increases logarithmically with $I_{D,str}$ and linearly with $V_{DS,str}$, due to the higher amount of injected hot carriers, as well as due to the higher electric field and therefore higher kinetic energy. At higher $V_{DS,str}$ the slope of the curves increases, indicating that the degradation depends on the drain bias level, as also reported in [12].

3.3. Recovery analysis

From the recovery transients as e.g. in Fig. 5(b) the time constants, τ, are extracted and plotted as a function of the gate voltage during recovery $V_{GS,rec}$ (Fig. 7(a)) for different temperatures (see solid lines). The time constant is determined from the time instant where the current transient reaches $\left(1-\frac{1}{e}\right)$ of its value. Fig. 7(b) shows the same data as a function of recovery gate current $I_{G,rec}$. The gate current has been obtained using the I_G-V_{GS} curve in Fig. 2(b). From the graphs in Fig. 7(a, b) it is possible to distinguish two regimes: (i) gate voltage/current independent, thus purely thermally driven regime which dominates for V_{GS} < 3 V and (ii) gate voltage/current dependent regime for V_{GS} > 3 V where the temperature dependence is weaker. From the $\tau(V_{GS})$ data in Fig. 7(a) at V_{GS} = 2 V (i.e. in the thermally-driven recovery regime) the Arrhenius plot is extracted for two different devices (Fig. 7(c)). The derived activation energies of 0.79 eV and 0.82 eV suggest a relation to carbon defects [13]. Recent studies indicate that the thermal activation of negative charge neutralization at the carbon defect can be governed by hole transport in GaN valence or defect bands, depending on carbon concentration [15,16]. In this model the time constant of the hole transport dominates over the time constant of the hole capture on the defect [15].

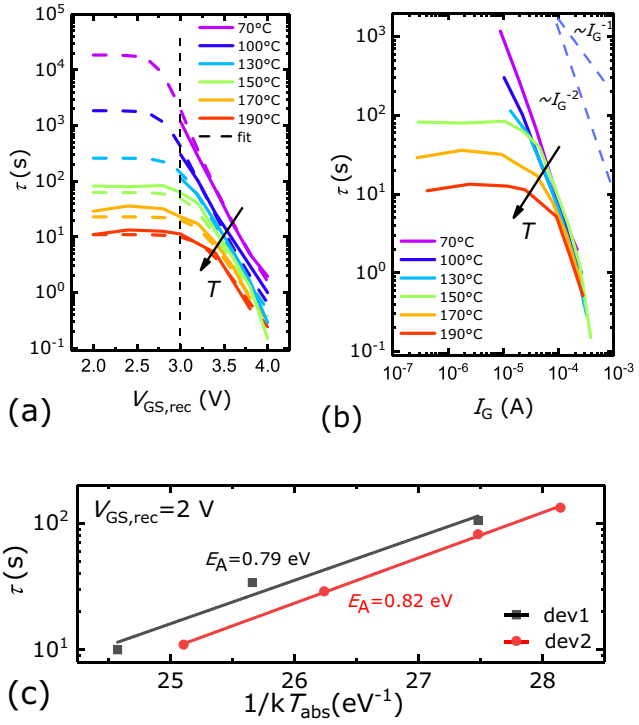

Fig. 7. Extracted recovery time constants τ as a function of the (a) gate voltage $V_{GS,rec}$ and (b) gate current I_G for different temperatures. The solid lines in (a) represent the experimental data, while the dashed lines highlight the fitting $\tau_{tot}(V_{GS})$ for $B = 1.7 \times 10^{-7}$ (1/sA^2) according to Eq.(4). (c) Arrhenius plot extracted from the data of (a) for V_{GS} = 2 V (thermally-driven recovery regime). T_{abs} is the absolute temperature.

In the gate-voltage limited regime at V_{GS} > 3 V we observe a roll-off of the $\tau(I_G)$ dependence which has a form of $I_G{}^{-2}$ (Fig. 7(b)). Similarly as in [9,10], we suppose that holes injected from the p-GaN into the buffer are captured to the same negatively charged defects, thus neutralizing them and leading to recovery of the drain current.

We propose a simple model in order to explain the thermally-driven and hole-induced recovery. We consider the following kinetic equation for the decay of concentration N of the negative trapped charge, which is the cause of the current collapse:

$$\frac{dN}{dt} = -\frac{N}{\tau_{temp}} - A \times p(I_G) \times N = -\frac{N}{\tau_{tot}(I_G)}, \quad (2)$$

where τ_{temp} is the time constant related to the thermally-driven regime for V_{GS} < 3 V (Fig. 7(a, b)), A is the capture rate constant and p the hole concentration. The first and second term in (2) represent the thermally-driven and hole-induced concentration decay terms. We emphasize that the time constant τ_{temp} is attributed to the already-mentioned temperature dependence of transport of background holes in the GaN buffer valence or defect bands [15]. On the other hand, holes with concentration p are additionally injected from the gate into the buffer. τ_{tot} is thus the total time constant which can be compared to the measurements in Fig. 7(a):

$$\tau_{tot} = \frac{1}{\frac{1}{\tau_{temp}} + A \times p}. \quad (3)$$

It would be natural to consider that p is proportional to I_G, so τ in the region V_{GS} > 3 V would be proportional to $I_G{}^{-1}$. However, the data shows that the slope of the roll-off region is −2. We have thus tentatively fitted the data of $\tau(V_{GS})$ using the following equation:

$$\tau_{tot}(T, V_{GS}) = \frac{1}{\left[\frac{1}{\tau_{temp}}(T) + B \times I_G{}^2(T, V_{GS})\right]}, \quad (4)$$

where B is the same common fitting constant for all temperatures. The result of the fittings is given by dashed lines in Fig. 7(a). The longer time constants for the region V_{GS} < 3 V, which are out of the experimentally feasible time range, are obtained by extrapolating the Arrhenius diagram of Fig. 7(b) to low temperatures. Even if the experimental data can be reasonably fitted with Eq. (4), the physical nature behind is yet unclear. In order to explain the $\tau \sim I_G{}^{-2}$ dependence for V_{GS} > 3 V one would need to consider the ideality factor of the I_{GS}-V_{GS} dependence in the 3–4 V range being twice lower than the one measured in Fig. 2(b).

Among several hypotheses to explain this slope inconsistency we discuss here only few of them: (i) The gate current I_G can be considered as the sum of hole and electron components which have different ideality factors. One would need to consider that the electron current component dominates in the range 3–4 V and has ideality factor of 4–5 (see part 2), while the hole current component is negligible and has ideality factor 2–2.5. The dominance of the electron current component is however unlikely since the valence band discontinuity between p-GaN and AlGaN is lower than the conduction band discontinuity [17].

In turn the hole current likely dominates the gate current which contradicts the above assumption. (ii) The capture coefficient A in (3) can depend on p, but the physical reason is not known. Maybe the injected holes in the buffer modify the potential in the GaN buffer in such a way that the hole capture term in (3) has the form as in (4). (iii) For an unknown reason the hole concentration p is dependent on square of I_G instead of linearly proportional. (iv) We also think that series resistance effects as, e.g. due to possibly rectifying property of the p-GaN/contact metal junction, cannot explain the I_G^{-2} roll-off of the $\tau(I_G)$ data, since the series resistance does not influence it.

Understanding this behavior is a topic of further investigations.

4. Conclusions

Stress and recovery drain current transients have been analysed in GaN HD-GITs under semi-ON stress. For the same stress current the drain current degradation is lower at higher stress temperatures which can be attributed to less hot carriers available for trapping or partial recovery during the stress. The recovery shows a pure thermally-driven recovery for $V_{GS} < 3\,V$ and gate-current induced recovery for $V_{GS} > 3\,V$. A tentative model has been proposed to unify both recovery mechanisms in a single equation.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgements

This work was funded by the Austrian Research Promotion Agency (FFG, Project No. 874907).

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