Microelectronics Reliability 100–101 (2019) 113331

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Effect of TLP rise time on ESD failure modes of collector-base junction of SiGe heterojunction bipolar transistors

Clément Fleury[a,b,*], Werner Simbürger[c], Dionyz Pogany[a,**]

[a] Institute for Solid State Electronics, TU Wien, Gusshausstrasse 25, 1040 Vienna, Austria
[b] Carinthian Tech Research AG, Europastrasse 12, 9524 Villach, Austria
[c] Infineon Technologies AG, 85579 Munich, Germany

A B S T R A C T

Electrostatic discharge behavior of integrated SiGe heterojunction bipolar transistors is investigated by transmission line pulse (TLP) and transient interferometric mapping techniques. When stressing collector - base junction in reverse direction, two distinct non-thermal failure modes, depending on TLP pulse rise time (RT), have been found: For RT ≥ 10 ns the observed failure at a critical voltage is attributed to base corner breakdown as supported by failure analysis. For RT ≤ 5 ns the failure occurs due to parasitic capacitance coupling which virtually short-circuits the base-emitter junction at the pulse beginning and thus induces a parasitic bipolar action.

1. Introduction

Discrete SiGe heterojunction bipolar transistors (HBTs) are widely used in RF amplifiers for telecommunication and mobile applications in the frequency range of 0.6–6 GHz [1]. During the amplifier assembly the HBT devices are subjected to various disturbing pulses as electrostatic discharge (ESD) [2]. Human body model ESD robustness of 1 kV [3] and charged device model robustness of 300–500 V [4] are typically required. ESD behavior of SiGe HBTs has been studied in different configurations [5–8]. Usually the reverse biased base-collector (BC) junction is the most vulnerable junction due to highest voltage and thus highest power dissipation on it. Power to failure has been studied in [7], showing a thermal failure according to Wunsch-Bell behavior [9].

This works investigates ESD behavior of reverse-bias stressed collector-base junctions of SiGe HBTs of 0.35 µm bipolar process. TLP analysis is combined with imaging of finger activity by transient interferometric mapping (TIM) [10]. Two non-thermal modes of failure have been found depending on TLP pulse rise time (RT). The failure mode at long RT (10 ns) is found to be due to breakdown at the base corner. At short RTs (≤5 ns), the failure is attributed to virtual short-circuiting of the base-emitter junction caused by capacitance coupling effect and thus activation of parasitic bipolar action leading to destructive current filamentation.

2. Devices and experiments

Studied HBTs are composed of n-doped buried collector layer (NBL), about 75 nm thick epitaxial Si_xGe_{1-x} (x = 0.85) p-doped base and highly n-doped epitaxial and polysilicon emitter. Simplified schematics of the cross section of one HBT finger (i.e. a half of a double finger) including metallization layers and contacts is given in Fig. 1a. The top layout of a device composed of 16 active double fingers (labeled here as 32F device) is given in Fig. 1b. For simplicity, the metal lines for contacting base, emitter and collector regions are indicated only in selected fingers. In the 32F device the emitter is connected to the substrate by top metallization. The lumped element representation of this device with parasitic substrate diode D and parasitic base, R_B, and collector, R_C, resistances is given in Fig. 1c. The emitter resistance is negligible. The emitter length L_E was 20 µm and the emitter width W_E = 0.5 µm. Test structures of single double finger devices (labeled 2F), with separate emitter and substrate contacts, were also investigated, with L_E = 20 µm and W_E ranging 0.35 µm to 1.8 µm.

The TLP characterization has been performed with a HPPI pulser [11] in 4 - point configuration with pulse RTs of 300 ps, 1 ns, 5 ns and 10 ns. TLP pulse width (PW) was in the range 20–400 ns.

For the analysis of dissipated power along the device fingers, TIM technique [10] has been used. The measured optical phase shift is proportional to areal density of thermal energy [12]. Although the photon energy of the probing laser beam (0.95 eV for wavelength of 1.3 µm) is above the band bap of SiGe, the resulting small photocurrent

* Corresponding author at: Carinthian Tech Research AG, Europastrasse 12, 9524 Villach, Austria.
** Correspondence to: D. Pogany, Institute for Solid State Electronics, TU Wien, Gusshausstrasse 25, 1040 Vienna, Austria.
E-mail addresses: clement.fleury@ctr.at (C. Fleury), dionyz.pogany@tuwien.ac.at (D. Pogany).

https://doi.org/10.1016/j.microrel.2019.06.023
Received 15 May 2019; Accepted 12 June 2019
Available online 23 September 2019

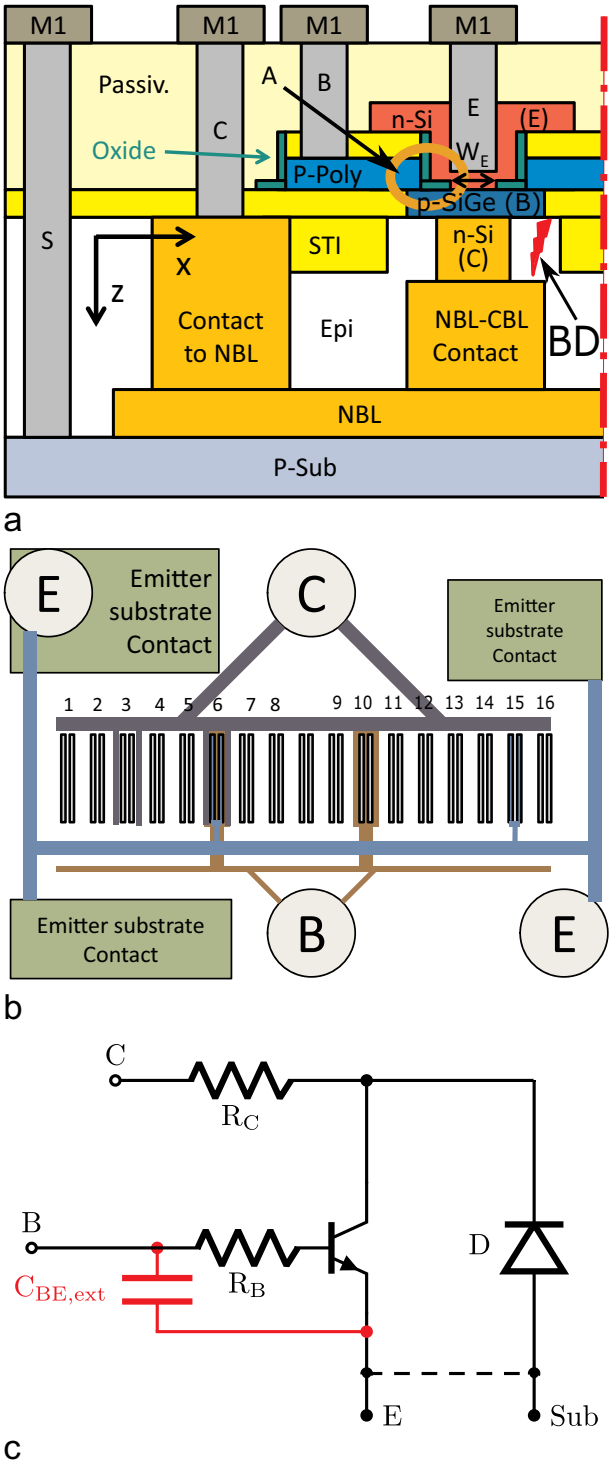

Fig. 1. (a) Simplified cross section of a half of a double finger of the studied devices. The base corner to collector breakdown is indicated by "BD". The base to emitter overlap region causing parasitic $C_{B,EXT}$ is indicated by "A". (b) Simplified layout of 32F device with 16 double-fingers. (c) Lumped element representation of the HBT with the main considered parasitic elements: RB - base resistance which includes both intrinsic and extrinsic parts; RC - effective collector resistance composed of NBL and NBL-contact resistances (cf. (a)); D - NBL to p-substrate diode, $C_{BE,EXT}$ – base to emitter parasitic overlap capacitance of region A from (a). The emitter and substrate (SUB) contacts are short - circuited in 32F device.

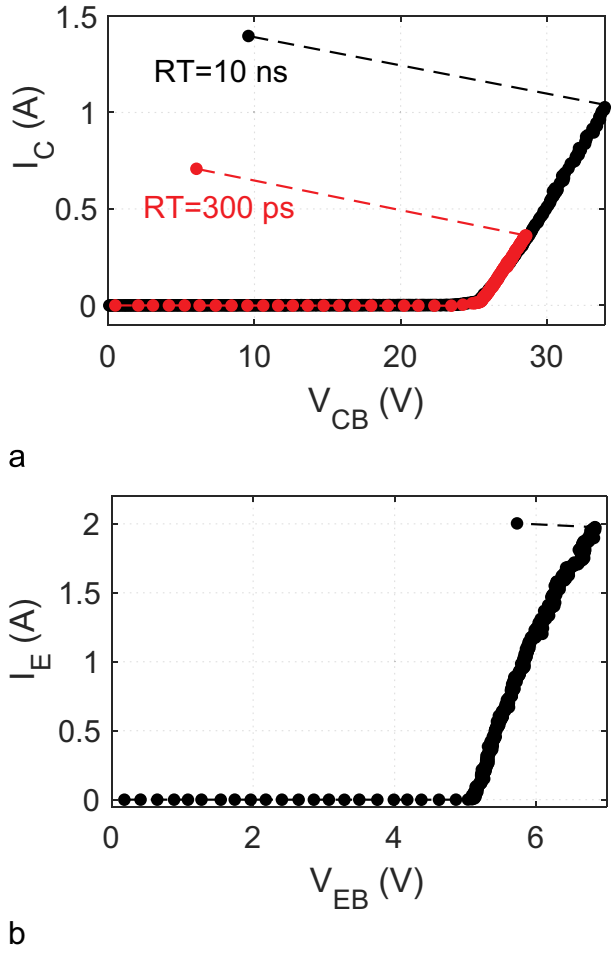

Fig. 2. 100 ns TLP IV characteristics of 32F device for (a) reverse-biased CB junction at two different rise times and (b) reverse-biased EB junction at RT = 10 ns. The averaging window is 70–90% of the pulse width. The ON resistance of the I_C (V_{CB}) curve in (a) is dominated by R_C.

due to absorption in the thin base layer was found to have negligible influence of the triggering behavior of the device and its failure current I_{T2}. TIM measurements were performed at wafer level, using the same TLP setup with microwave probes, but only in two-point configuration.

3. Results and discussion

3.1. General behaviour

Typical 100 ns TLP IV characteristics of reverse biased CB junction of the 32F device for two different rise times are given in Fig. 2a. While for RT = 10 ns the failure current I_{T2} is 1A, for RT = 300 ps the I_{T2} is about 0.35 A. By stressing devices with different rise times we have found that the I_{T2} varies in the 0.3–0.7 A range for RT ≤ 5 ns. Typical current and voltage waveforms just before and at the failure for the RT = 10 ns and RT = 300 ps are given in Fig. 3a and b, respectively. The device failure exhibits itself as a sudden drop in voltage. While for RT = 10 ns, the device can fail at any time during the pulse duration (in Fig. 3a it is close to the pulse end), for RT = 300 ps the failure occurs at the pulse beginning (Fig. 3b). The same type of failure, i.e. occurring at the pulse beginning, is observed also for other rise times up to 5 ns.

The differential resistance of the reverse-biased CB junction (Fig. 2a) is a sum of R_C and R_B as can be seen from Fig. 1c. To distinguish between the R_B and R_C we have also performed characterization of reverse biased EB junction, see Fig. 2b. The differential resistance of the reverse-biased EB junction is mainly due to the base resistance R_B

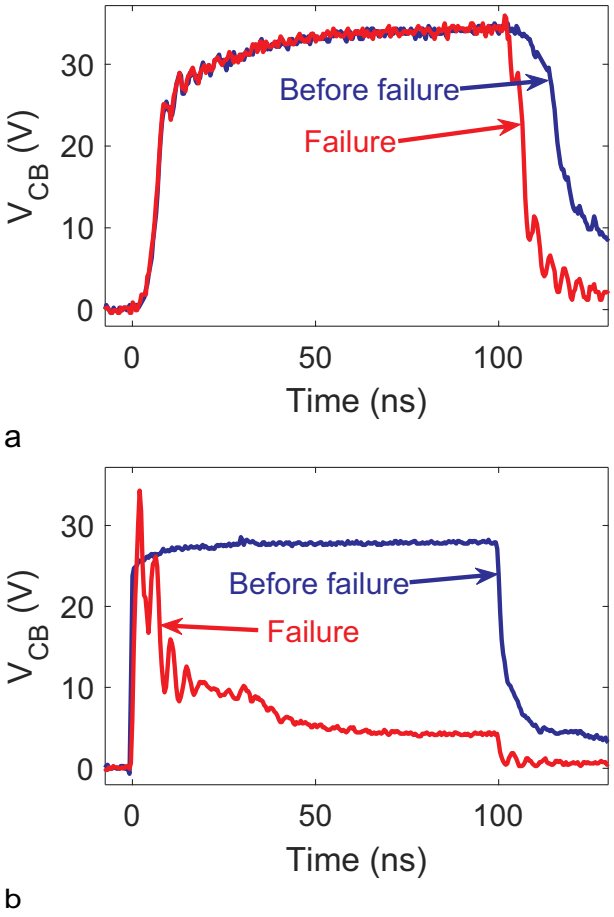

Fig. 3. Typical voltage and current waveforms of the reverse-biased CB junction in 32F device just before and during the failure for (a) RT = 10 ns and (b) RT = 300 ps. The peaks in the voltage waveform at the failure in (b) are artifacts and do not represent the actual voltage on the device.

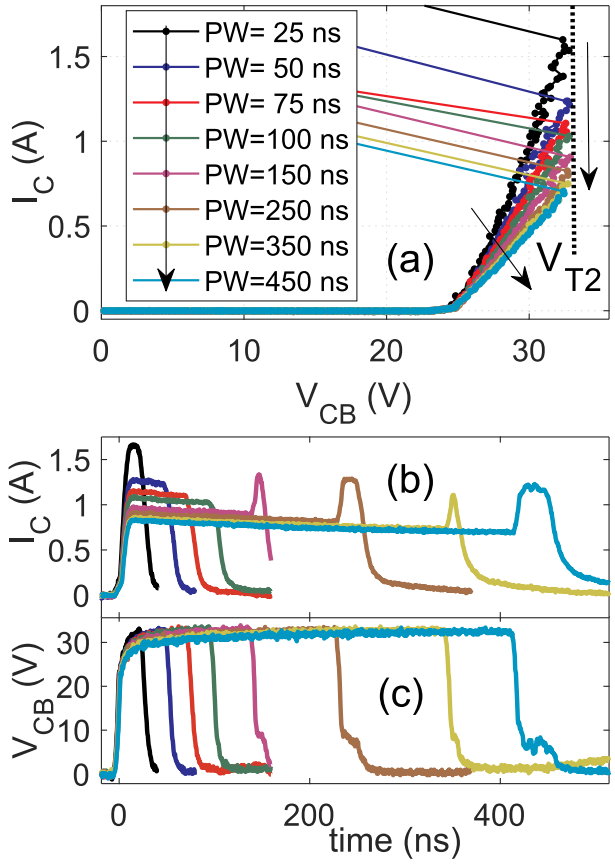

Fig. 4. (a) Current and (b) voltage waveforms for different pulse durations in reverse-bias stressed CB junction of 32F device. The charging voltage was chosen so that the failure moment is captured; (c) corresponding TLP IV curves as a function of pulse width PW; RT = 10 ns. The averaging window is 70–90% of the pulse width.

which is estimated to be 1 Ω. Thus R_C of ≈7 Ω can be deduced by analyzing the CB and EB TLP IV data in Fig. 2a and b, respectively. R_C is composed of the effective resistance of the collector buried layer NBL and the NBL-contact resistance, see Fig. 1a. The breakdown voltage V_{BD} of the CB junction of about 25 V is higher compared to V_{BD} ≈ 5.2 V of the EB junction since the latter junction is highly doped. The I_{T2} of EB junction (2A) is twice higher than that of the CB junction for RT = 10 ns, but it does not scale proportionally with the applied power. This is because in the case of CB stressing a large part of power is dissipated in semiconductor bulk compared to a small active volume around thin epitaxial base in the case of EB stressing.

In the next two subsections we investigate the origin of reverse biased CB junction failures for RT = 10 ns and RT ≤ 5 ns.

3.2. Failure mode for RT = 10 ns

3.2.1. TLP analysis

Fig. 4a and b show typical current and voltage waveforms for the 32F device for different pulse durations and RT = 10 ns. The charging voltage is chosen so that the moment of device failure (i.e. voltage drop) is visible at the pulse end. Fig. 4c shows the corresponding TLP IV curves for different PW. The extracted I_{T2}, V_{T2}, differential resistance R_{ON} and power at failure as a function of PW are given in Fig. 5a–d respectively.

Fig. 5b shows that the device fails at constant V_{T2} of 33 V which indicates a non-thermal failure mechanism. Fig. 5d shows that power to failure data have power exponent coefficient of (−0.17) confirming that this failure mode is non-explainable by any known thermal failure models of Wunsch-Bell [9] or Dwyer [13] where the power exponent is −0.5 or −1. This power exponent of −0.17 is an apparent effect of constant V_{T2} and decreasing I_{T2} with increasing pulse width.

The increase in R_{ON} in Figs. 4c and 5c is attributed to the self-heating effect. R_{ON} increases during the TLP pulse which is seen as a voltage increase during the TLP pulse plateau in Fig. 4b. When a critical voltage of 33 V is reached, the device fails.

Fig. 6 shows the 100 ns TLP IV curves of the 2F devices with W_E as parameter. For these experiments the emitter was connected to the substrate externally to mimic the conditions in the 32F device. V_{T2} increases with W_E until W_E = 0.7 μm and then saturates at 33 V (see the inset of Fig. 6) which shows again the voltage-limited failure behavior.

3.2.2. TIM analysis

Fig. 7a shows a TIM scan across one double finger of a 32F device at I = 0.6 A. The temperature-induced phase shift shows a main peak at the position of the two emitters and two side peaks at the collector contacts. The central peak is due to power dissipation at the BC junction plus a contribution from the NBL-contact, while the side peaks indicate power dissipation at the collector access resistance R_C due to NBL and NBL-contacts. Thus the power sharing between the BC junction and R_C resistance is demonstrated (c.f. the TLP IV curve 1 in Fig. 2a for RT = 10 ns). The power dissipation along the emitter length (i.e. the longer device lateral dimension) has been found homogeneous (not shown).

Fig. 7b shows a TIM scan at the equivalent position of the peaks in the 16 active double fingers, demonstrating a homogeneous power

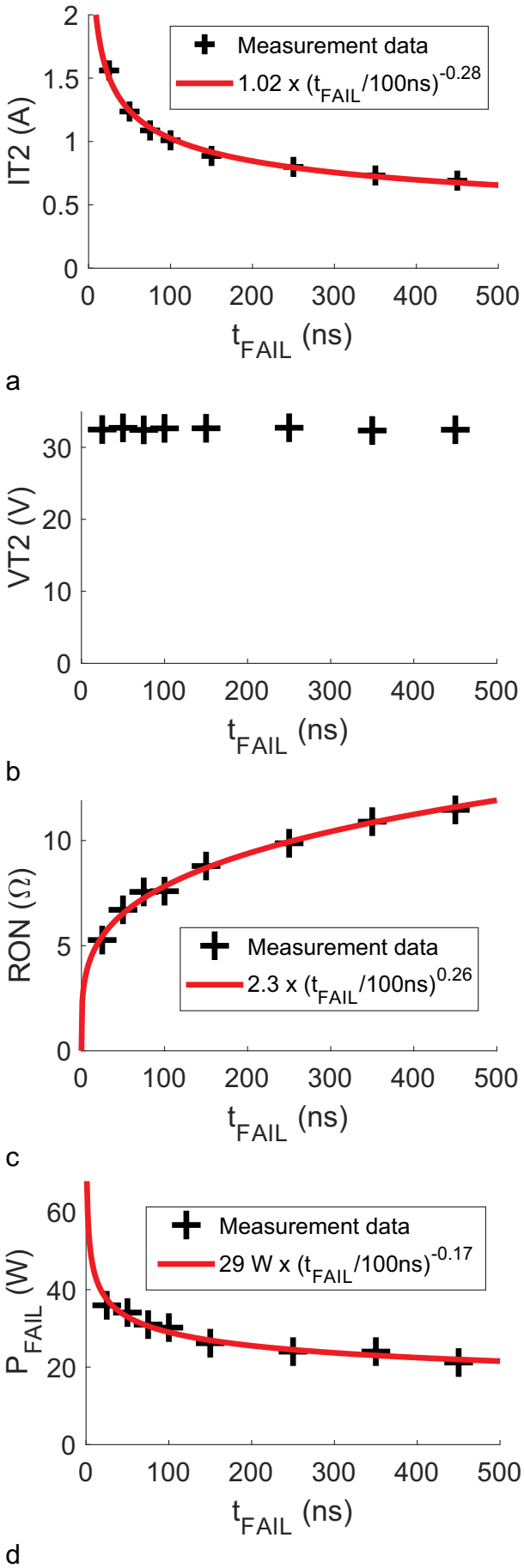

Fig. 5. Extracted parameters from the analysis of TLP data of the reverse biased BC junction of the 32F device of Fig. 4: (a) IT2, (b) VT2, (c) RON for 70–90% of the pulse width as averaging window and (d) power to failure as a function of time-to-failure. In (d) the failure power is calculated as averaged power from the I (t) and V (t) curves up to the failure moment; RT = 10 ns.

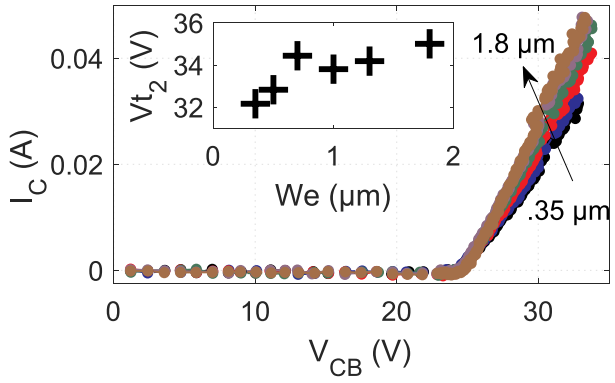

Fig. 6. 100 ns TLP IV characteristics of the reverse-biased stressed CB junction of 2F devices for different WE parameter. Inset: failure voltage VT2 as a function of WE; RT = 10 ns.

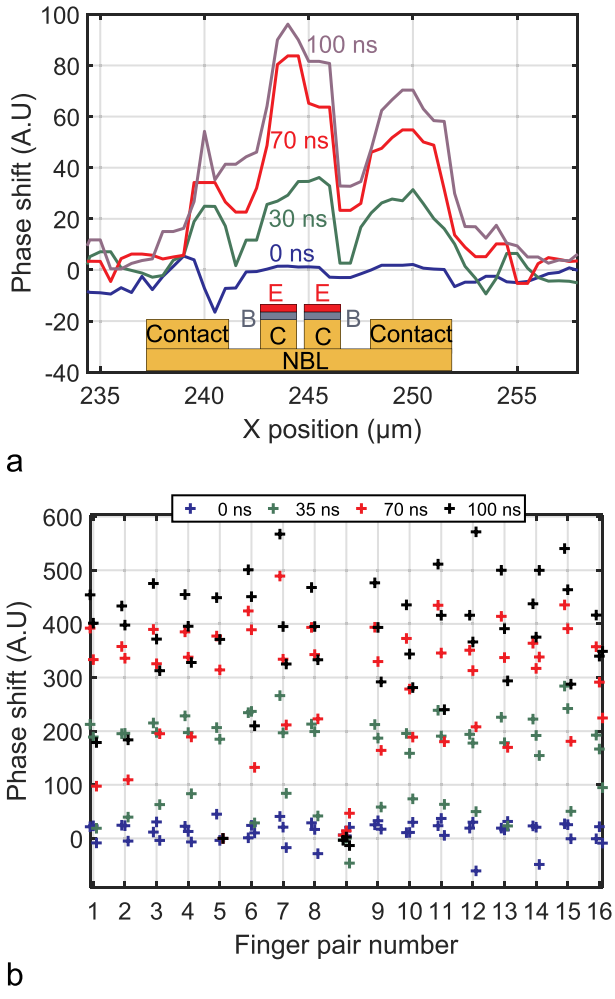

Fig. 7. TIM experiments in a 32F devices for I = 0.6A in the reverse-bias stressed CB configuration. Time during a 100 ns long TLP pulse is parameter. The scanning position is in the middle of finger (s): (a) detailed scan across one double finger; (b) TIM-phase values in the middle of a double finger (cf. (a)) for 16 active double fingers. The middle double finger is not contacted; RT = 10 ns.

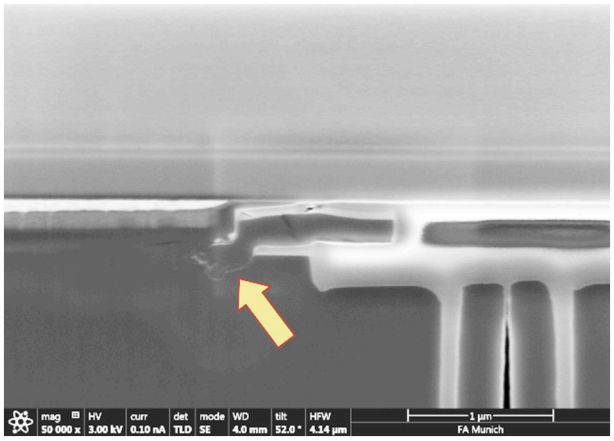

Fig. 8. SEM image of a failed 2F device at the position of failure crack. The arrow indicates the base corner damage as the origin of voltage-limited failure mode at RT = 10 ns (see "BD" in Fig. 1a for failure localization).

sharing between the fingers. In total there is no sign of a hot spot, at least for the geometry and stress conditions that were investigated.

3.2.3. Failure analysis

For physical failure analysis, a 2F device has been chosen which exhibited only a small increase in CB leakage current after failure (500 pA compared to <10 pA at 1 V reverse bias before the stress). In this device the failure occurred close to the pulse end at 33 V, so the device was not stressed a long time in the failed state. We notice that the normalized failure current in the 2F and 32F device is the same: 1.5 µA/µm. Such a weak damage was suitable for failure localization by thermally induced voltage alteration (TIVA) technique [14]. Furthermore, sequential focused ion beam cross sectioning and the scanning electron microscopy (SEM) have been used to find the exact failure location. The SEM image on Fig. 8 shows a crack at the corner of the base epitaxial region (see the arrow). We suppose that due to high electric field at the sharp base corner, a breakdown between the base corner and the buried collector regions occurs (see "BD" in Fig. 1c). This breakdown voltage (33 V) is clearly independent of the layout parameters, in accordance with the results of Figs. 5b and 6. The weak increase of V_{T2} with We in Fig. 6 is attributed to the rise of the voltage on the contact resistance, as a wider emitter involves a higher current due to the related design variations.

3.3. Failure mode for RT ≤ 5 ns

We suppose that this failure mode resembles to failure of reverse-biased BC junction with short-circuited base and emitter where parasitic capacitive action between the base and emitter plays a decisive role. We consider that for short rise times the extrinsic BE capacitance $C_{BE,EXT}$ (Fig. 1c) virtually short-circuits the B and E terminals at position A indicated in Fig. 1a. This is feasible because $C_{BE,EXT}$ likely dominates other overlap capacitances. As a result, the emitter potential at point A will follow the base potential at the same location during the short pulse rising edge. When the avalanche multiplication in the BC junction starts, the holes from the collector move vertically toward the base layer and then laterally in the p-base toward the base contact.

The resulting lateral potential drop on the base resistance R_B and the virtually short – circuited BE junction causes a similar situation as in a grounded gate MOSFET [2] and thus activates the parasitic bipolar action. As the device enters the negative differential resistance region of the IV curve, destructive current filaments are quickly formed and destroy the device.

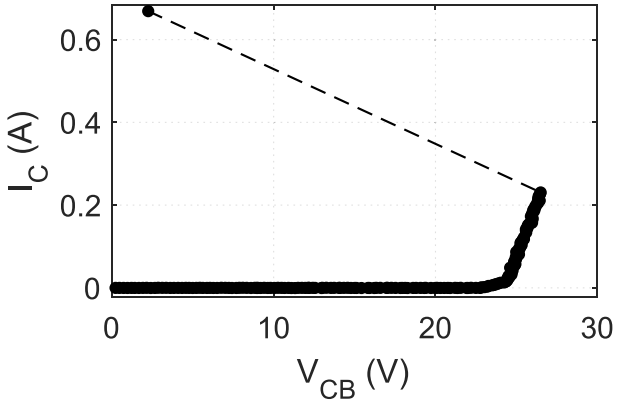

Fig. 9. 100 ns TLP IV curve for the reverse-biased CB junction with *short-circuited* base and emitter contacts in 32F device; RT = 10 ns.

To support this hypothesis, we have first examined the extreme case where the base and emitter are short-circuited. Fig. 9 shows the TLP IV curve under the condition where E and B contacts are externally short-circuited by a short between the needles of a coaxial probe. Typical current and voltage waveform at failure are qualitatively similar as for the failure mode for RT ≤ 5 ns (see Fig. 3b). The failure current is 0.25 A. Here the failure is due to the potential drop on the base resistance R_B (see Fig. 1c). Taking $R_B = 1\ \Omega$, the potential drop of 0.25 A * 1 Ω = 0.25 V at the forward-biased BE junction is thus already expected to activate the parasitic bipolar action. We notice that within the above hypothesis, the I_{T2} of 0.25 A for the short-circuited B and E contacts represents the lower bound for I_{T2} for failure mode for RT ≤ 5 ns.

To further support the existence of parasitic bipolar action at such low forward BE voltage V_{BE} we have examined how I_{T2} depends on an externally applied V_{BE}, see Fig. 10a. In these experiments a 10 nF capacitor has been placed as close as possible to the E and B contacts to reduce possible parasitics (Fig. 10b). The voltage appearing at the BE junction is thus the sum of applied V_{BE} voltage and the potential drop I * R_B on the R_B resistance. The value of I_{T2} for $V_{BE} = 0$ V is in between 0.25 and 0.3 A (Fig. 10a) which is consistent with the I_{T2} value found from the measurements with the short-circuited BE contacts (Fig. 9). The decrease in I_{T2} under forwardly-biased BE junction in Fig. 10a shows that the part of electrons injected from the emitter through the base can be multiplied in the collector, thus activating parasitic bipolar transistor action leading to voltage snapback behavior. This strongly supports the failure hypothesis proposed at the beginning of this paragraph. No failure analysis could be performed on the devices that were damaged with this failure mode, as the energy could not be limited to values that would create a damage signature worth analyzing. Other stressing modes such as very fast TLP could be used for this purpose.

4. Conclusions

The studied SiGe HBTs exhibit two distinct non-thermal failure behaviors of the reverse – bias stressed BC junction, depending on TLP pulse rise time. For long rise times (RT ≥ 10 ns) the device exhibits a voltage-limited failure at a critical voltage of 33 V. The failure analysis revealed damage at the base corner, which indicates that the failure occurs when a critical breakdown voltage between the corner and buried collector is reached. For short rise times (RT ≤ 5 ns) the failure is due to due to virtual short-circuiting of the base and emitter terminals by a parasitic capacitance which occurs at the pulse beginning. The resulting parasitic bipolar action leads to the formation of destructive

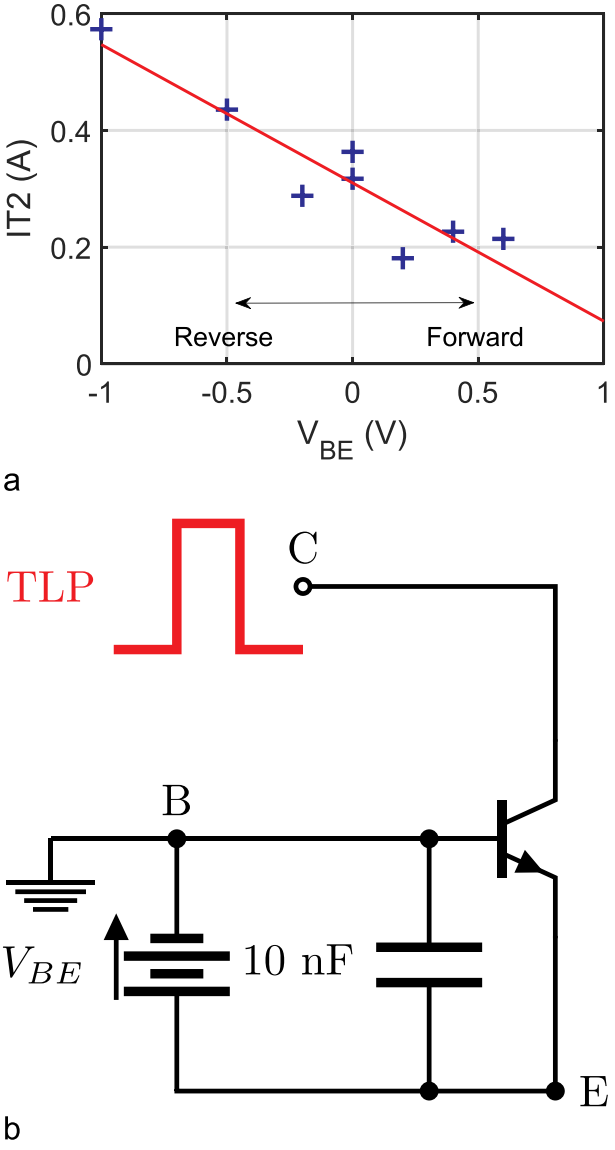

Fig. 10. (a) IT2 of the reverse-biased CB junction as a function of externally applied emitter - base voltage VBE; RT = 10 ns @ PW = 100 ns (b) corresponding schematics of the measurement configuration.

current filaments. This type of failure is not critical to HBM or CDM robustness in the current designs but poses limits on the current mitigation strategies for the development of future ESD self-protection schemes. Designing the sub-collector region for high parasitic breakdown and limiting the BE capacitance should increase the robustness of SiGe-HBTs.

References

[1] J. Cressler, SiGe HBT technology: A new contender for si-based RF and microwave circuit applications, IEEE Transactions on Microwave Theory and Techniques, 46 may 1998, pp. 572–589.
[2] A. Amerasekera, C. Duvvury, ESD in Silicon Integrated Circuits, John Wiley & Sons, Ltd, 2002 apr.
[3] I. EOS/ESD Association, ANSI/ESDA/JEDEC JS-001-2014- ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing-Human Body Model (HBM) - Component Level, EOS/ESD Association, Incorporated, 2014.
[4] I. EOS/ESD Association, ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing-Charged Device Model (CDM) - Device Level, EOS/ESD Association, Incorporated, 2014.
[5] C. Chou, S. Chen, T. Tang, ESD investigation of pn junction diodes in silicon-germanium heterojunction bipolar transistor, Electron. Lett. 39 (14) (2003) 1089.
[6] S. Voldman, P. Juliano, R. Johnson, N. Schmidt, A. Joseph, S. Furkay, E. Rosenbaum, J. Dunn, D. Harame, B. Meyerson, Electrostatic discharge and high current pulse characterization of epitaxial-base silicon-germanium heterojunction bipolar transistors, 2000 IEEE International Reliability Physics Symposium Proceedings. 38th Annual (Cat. No.00CH37059), IEEE, 2000.
[7] S. Voldman, P. Juliano, N. Schmidt, A. Botula, R. Johnson, L. Lanzerotti, N. Feilchenfeld, J. Joseph, J. Malinowski, E. Eld, V. Gross, C. Brennan, J. Dunn, D. Harame, D. Herman, B. Meyerson, ESD robustness of a BiCMOS SiGe technology, Proceedings of the 2000 BIPOLAR/BiCMOS Circuits and Technology Meeting (Cat. No.00CH37124), IEEE, 2000.
[8] S. Voldman, A. Botula, D. Hui, and P. Juliano, "Silicon Germanium Heterojunction Bipolar Transistor ESD Power Clamps and the Johnson Limit," pp. 324 – 334, vol. 10 2001.
[9] D.C. Wunsch, R.R. Bell, Determination of threshold failure levels of semiconductor diodes and transistors due to pulse voltages, IEEE Trans. Nucl. Sci. 15 (6) (1968) 244–259.
[10] M. Litzenberger, C. Furbock, S. Bychikhin, D. Pogany, E. Gornik, Scanning heterodyne interferometer setup for the time-resolved thermal and free-carrier mapping in semiconductor devices, IEEE Trans. Instrum. Meas. 54 (dec 2005) 2438–2445.
[11] W. Simbürger, D. Johnsson, M. Stecher, High current tlp characterisation: An effective tool for the development of semiconductor devices and esd protection solutions, ARMMS, RF & Microwave Society, 2012 (9th to 20th November 2012 at Wyboston Lakes, Wyboston, UK (invited).
[12] D. Pogany, S. Bychikhin, C. Furbock, M. Litzenberger, E. Gornik, G. Groos, K. Esmark, M. Stecher, Quantitative internal thermal energy mapping of semiconductor devices under short current stress using backside laser interferometry, IEEE Transactions on Electron Devices 49 (nov 2002) 2070–2079.
[13] V. Dwyer, A. Franklin, D. Campbell, Thermal failure in semiconductor devices, Solid State Electron. 33 (May 1990) 553–560.
[14] J.M. Soden, R.E. Anderson, IC failure analysis: techniques and tools for quality and reliability improvement, Microelectron. Reliab. 35 (mar 1995) 429–453.