INFOS 2019
will be held on 30th June - 3rd July 2019
at Clare College,
Cambridge University, Cambridge, UK

INFOS 2019

The INFOS conference is a 2-yearly event, bringing together electrical engineers, materials scientists, physicists and chemists to debate the latest developments in semiconductors and insulating films for CMOS devices, memory devices, and processing, as devices scale ever smaller and denser. The conference will be over 3 days, with a welcome reception and social events on the previous day (Sunday).

INFOS 2019, Clare College, Cambridge University, UK

Program

Sunday 31 June 2019

Welcome Reception

18:00 - 20:30 The Scholars Garden - drinks (prosecco / soft drinks) and nibbles.

Monday 1 July 2019

Session 1: Steep Slope Devices

9:00 1.1 S. Datta, **(Plenary)** *Penn State University, USA*, Overcoming the Boltzmann Tyranny in Steep Slope Devices.

9:45 1.2 A H Ionescu, (Invited) *EPFL, Switzerland*, Steep Slope Devices with Active Gates for Electronic Functions Near-100 millivolts.

10:45 Coffee Break

Session 2: Negative Capacitance and Ferroelectric HfO_2 I

10:45 2.1 S Sleszazeck, (Invited) *NAMLAB, Dresden, Germany*, Switching Kinetics in Hafnium Oxide-based Ferroelectric / Dielectric Bilayer Stacks.

11:15 2.2 Min-Hung Lee, (Invited) *National Taiwan Normal University, Taipei, Taiwan*, Ferroelectric $HfZrO_2$ FETs for Steep Switch Onset.

11:45 2.3 Peide Ye, (Invited) *Purdue University, USA*, Ferroelectric and Anti-ferroelectric $HfZrO_2$: Scaling Limit and Switch Speed.

12:15 2.4 C. Zacharaki*, P. Tsipas1, S. Chaitoglou1, S. Fragkos1, L. Pintilie3, R. Negrea3, A. Dimoulas1, *Demokritos, Athens*, TiN/ZrxHf1-xO2/Ge Metal-Ferroelectric-Semiconductor Capacitors by Plasma Assisted Molecular Beam Deposition.

Wednesday 3 July 2019

Session 9: Atomic Layer Deposition and Etching

9:00 9.1 P Chalker (Invited), *Liverpool University, UK*. Atomic-layer Engineering of Ultrathin Dielectric Films.

9:30 9.2 C Hinkle (Invited), *University of Notre Dame, IN, USA*, Vertical Integration Through Direct Growth of van der Waals Materials.

10:00 Coffee Break

Session 10A: 2D, Memory and Dielectric Materials

10:03 10A.1 E. Caruso1*, J. Lin1, S. Monaghan1, K. Cherkaoui1, F. Gity1, P. Palestri2, D. Esseni2, L. Selmi3, P. K. Hurley1 *Tyndall Institute, Cork, Ireland*, Investigating Electrically Active Defect Distributions in MOS Structures Based on Inelastic Tunneling Interaction with Border Traps and a Nonlocal Model for Interface Traps.

10:45 10A.2 Andrea Redaelli, *Micron Semiconductor, Italy,* Recent trends in semiconductor memories (Invited)

11:15 10A.3 E. Pérez1, D. Maldonado2, C. Acal3, J.E. Ruiz-Castro3, F.J. Alonso3, A.M. Aguilera3, F. Jiménez-Molinos2, Ch. Wenger1, J.B. Roldán2, IHP, *University of Granada, Spain*, Analysis of the Statistics of Device-to-Device and Cycle-to-Cycle Variability in TiN/Ti/Al:HfO2 /TiN RRAMs.

11:30 10A.4 Viktoria Ritter1, Jakob Genser1, Daniele Nazzari1, Ole Bethge2, Emmerich Bertagnolli1, and Alois Lugstein1, [1]*TU Wien, Vienna, Austria;* [2]*Infineon Austria, Villach*; Silicene Passivation by Few-Layer Graphene.

11:45 10A.5 A. Mazurak, J. Jasiński, B. Majkusiak, *Warsaw University of Technology, Warsaw, Poland*, Effect of Traps-to-Gate Tunnel Communication on C-V Characteristics of MIS Capacitors.

12.00 10A.6 Y. X. Fang1,2,3, C. Zhao1,2,3, *, C. Z. Zhao1,2,3, *, I. Z. Mitrovic 2, L. Yang4, W. Y. Xu5, *Liverpool University, UK, Xian Jiaotung University, Xian, China*, Bias-Stress Stability and Ra00diation Response of Solution-Processed AlOx Dielectrics Investigated by On-Site Measurements.

12.15 10A.7 L.A.H. Jones1, P. Das2,, T.P. Manzanera1, J.T. Gibbon1, R. Potter1, P.R. Chalker1, R. Mahapatra2, V.R. Dhanak1, I.Z. Mitrovic1,* *Liverpool University, National Institute*