REGISTER MACHINES OVER GROUPS

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Abstract
Register machines are a classic model of computing, often seen as a canonical example of a device manipulating natural numbers. In this paper, we define register machines operating on general groups instead. This generalization follows the research direction started in multiple previous works. We study the expressive power of register machines as a function of the underlying groups, as well as of allowed ingredients (zero test, partial blindness, forbidden regions). We put forward a fundamental connection between register machines and vector addition systems.

1. Introduction

Register machines are traditionally seen as a model of computing manipulating non-negative numbers. However, quite some time ago integer numbers were already considered as the base set for register contents [7]. Such machines are traditionally called blind as long as they do not allow testing registers for zero, except eventually testing all registers for zero at the end. The computational power of such blind register machines is inferior to that of "conventional" register machines over natural numbers [2]. If the register machine is not allowed to go below zero, but can neither explicitly test its registers for zero, it is called partially blind.

Even further, we need not restrict the definition of the model to numbers. For example, Section 3 of [2] gives a very general definition of register machines whose registers may contain elements of any set A. However, going this far up the abstraction scale loses too much structure: almost nothing can be said about such general constructs. In this paper, we focus on a level of abstraction which is in between the two: we consider register machines over finitely presented groups. This generalization comes in as a natural sequel to multiple previous works. For

example, [8] introduced integer vector addition systems by lifting the traditional restriction on the vectors to only contain non-negative components. Subsequently, [6] generalized P systems (compartmentalized multiset rewriting systems [14]) to allow multiplicities of objects to come from Abelian groups instead of just natural numbers. Finally, papers [2, 3] come back on the less general case of integer multiplicities and show a number of new properties of integer vector addition systems and blind register machines.

In this work, we define register machines over arbitrary finite families of groups, with or without zero test, as well as partially blind register machines, and register machines with forbidden regions (Section 3). Each of these ingredients is meant to generalize individual features which appear in the classic definition of register machines. We then study the computational power of the variants we define: we compare the generating and the accepting modes, single- and multi-register machines, vector addition systems with and without states (Section 4).

2. Preliminaries

In this paper, we use the symbols $\mathbb{R}$, $\mathbb{Z}$, and $\mathbb{N}$ to refer to the set of real numbers, integer numbers, and the set of natural numbers including 0.

For an alphabet V, by V^* we denote the free monoid generated from the elements of V under the operation of concatenation, i.e., containing all possible strings over V. The *empty string* is denoted by λ. The family of all recursively enumerable sets of strings is denoted by RE, the corresponding family of recursively enumerable sets of Parikh sets (vectors of natural numbers) and of number sets is denoted by $PsRE$ and NRE, respectively. For an extensive introduction to the theory of formal languages, we recommend [14, 15].

Given a set A, a total function $f : A \times A \to A$ is called a *binary operation* over A. We will use the infix notation afb to refer to $f(a, b)$, for $a, b \in A$. A relation over a set A is any subset $R \subseteq A \times A$. As for binary operations, we will also use the infix notation aRb for $(a, b) \in R$.

A relation $\leq \subseteq A \times A$ is a called a *total order* if the following statements hold for every three elements $a, b, c \in A$:

- *antisymmetry*: if $a \leq b$ and $b \leq a$ then $a = b$,
- *transitivity*: if $a \leq b$ and $b \leq c$ then $a \leq c$,
- *totality*: either $a \leq b$ or $b \leq a$.

For $a, b \in A$ and a total order $\leq$ on A, we will sometimes write $b \geq a$ as equivalent to $a \leq b$, and use $a < b$ ($a > b$) to denote that $a \leq b$ and $a \neq b$ ($a \geq b$ and $a \neq b$).

2.1. Groups and Group Presentations

A group is the structure $G = (G', \circ)$ where G' is the set of elements (the underlying set) and $\circ : G' \times G' \to G'$ a binary operation over G' satisfying the following properties (*group axioms*):

- *closure*: for any $a, b \in G'$, $a \circ b \in G'$,
- *associativity*: for any $a, b, c \in G'$, $(a \circ b) \circ c = a \circ (b \circ c)$,
- *identity*: there exists a (unique) element $e \in G'$, called the *identity*, such that $e \circ a = a \circ e = a$ for all $a \in G'$, and
- *invertibility:* for any $a \in G'$, there exists a (unique) element a^{-1}, called the *inverse* of a, such that $a \circ a^{-1} = a^{-1} \circ a = e$.

The group G is called *commutative* or *Abelian*, if for any $a, b \in G'$, $a \circ b = b \circ a$. A *subgroup* of the group $(G, \circ)$ is any group $(H, \circ)$ with $H \subseteq G$ and the same group operation $\circ$. For any element $b \in G'$, the order of b is the smallest number $n \in \mathbb{N}$ such that $b^n = e$ provided such n exists, and then we write $ord\,(b) = n$. If no such n exists, $\{b^n \mid n \geq 1\}$ is an infinite subset of G' and we write $ord\,(b) = \infty$. In the following, we will often use the same symbol G to refer both to a group and to its underlying set.

The definitions and examples from group theory we exhibit now follow the exposition given in [1] and [2], based on the notions in [9].

For any set B, the set B^{-1} is defined to contain the symbols representing the "inverses" of the elements of B, i.e., $B^{-1} = \{b^{-1} \mid b \in B\}$. B (not containing the identity) is called a *generator set* of the group G if every element a from G can be written as a finite product/sum of elements from $B \cup B^{-1}$, i.e., $a = b_1 \circ \cdots \circ b_m$ for $b_1, \ldots, b_m \in B \cup B^{-1}$. In this paper, we restrict ourselves to finitely presented groups, i.e., having a finite presentation $\langle B \mid R \rangle$ with B being a finite generator set and moreover, R being a finite set of relations among these generators. Informally, the group $G = \langle B \mid R \rangle$ is the largest one generated by B subject only to the group axioms and the relations in R. We will restrict ourselves to relations of the form $b_1 \circ \cdots \circ b_m = e$ with $b_1, \ldots, b_m \in B$; omitting the identity e we write $b_1 \circ \cdots \circ b_m$, which then is called *relator*.

Example 2.1 *$\mathbb{Z}$ is a special case of an Abelian group generated by 1 and its inverse -1, i.e., $\mathbb{Z}$ is the free group generated by $B = \{1\}$. $\mathbb{Z}^d$ is the Abelian group generated by the unit vectors $(0, \ldots, 1, \ldots, 0)$ and their inverses $(0, \ldots, -1, \ldots, 0)$. It is well known that every finitely generated Abelian group is a direct sum of a torsion group and a free Abelian group, where the torsion group may be written as a direct sum of finitely many quotient groups of the form $\mathbb{Z}/p^k\mathbb{Z}$, with p a prime and $k \in \mathbb{N}$, and the free Abelian group is a direct sum of finitely many copies of $\mathbb{Z}$.*

Remark 2.2 *In this paper, we will restrict ourselves to finitely generated groups, for which the word equivalence problem $u = v$ is decidable, i.e., there exists a decision procedure telling us whether $u \circ v^{-1} = e$ for two strings u and v. In this case, we call G* recursive *or* computable. *If the set of relators R in a presentation $\langle B \mid R \rangle$ of G is computable (recursive), we call this a computable (recursive) presentation. Clearly, any finitely presented group is computable.*

A *linearly* or *totally ordered group* is construct $(A, +, \leq)$ where $(A, +)$ is a group, $\leq \subseteq A \times A$ is a total order on A and, for any triple $a, b, c \in A$, the fact that $a \leq b$ implies that $c + a \leq c + b$ and $a + c \leq b + c$.

2.2. Register Machines

Register machines are well-known universal devices for computing (generating or accepting) sets of vectors of natural numbers. The article [11] is one of the reference works on the universality of register machines.

Definition 2.3 *A* register machine *is the construct* $M = (m, B, l_0, l_h, P)$*, where*

- m *is the number of registers,*
- B *is a set of labels bijectively labeling the instructions in the set* P*,*
- $l_0 \in B$ *is the initial label,*
- $l_h \in B$ *is the final label, and*
- P *is the set of instructions.*

The labeled instructions in P *can be of the following forms:*

- $p : (ADD(r), q, s)$*, with* $p \in B \setminus \{l_h\}$*,* $q, s \in B$*,* $1 \leq r \leq m$*.*
  Increment the value of register r *and non-deterministically jump to instruction* q *or* s*.*
- $p : (SUB(r), q, s)$*, with* $p \in B \setminus \{l_h\}$*,* $q, s \in B$*,* $1 \leq r \leq m$*.*
  If the value of register r *is not zero then decrement the value of register* r *(*decrement *case) and jump to instruction* q*, otherwise jump to instruction* s *(*zero-test *case).*
- $l_h : HALT$*.*
  Stop the execution of the register machine.

A register machine M can be seen as an accepting device, a generating device, or as a device computing functions or relations. In this paper, we will only consider the accepting and the generating cases. In the *accepting* case, the first k registers of M are designated as input registers, and are initialized to a k-vector of natural numbers v (the input vector). If there exists a computation of M starting with this initial configuration and reaching the HALT-instruction, then v is accepted by M. Without loss of generality, we may assume all registers to be empty at the end of the computation. On the other hand, in the *generating* case, a single initial configuration is fixed for all computations of M, the first k registers are designated as the output registers, and for every halting computation of M, the k-vector contained in the output registers in the halting configuration is said to be generated by M. Without loss of generality, we may assume all registers with indices greater than k to be empty at the end of the computation.

By $\mathcal{L}_{acc}(M)$ and $\mathcal{L}_{gen}(M)$ we denote the set of input vectors accepted respectively generated by the register machine M. Similarly, for a family $\mathcal{X}$ of register machines, $\mathcal{L}_{acc}(\mathcal{X})$ and $\mathcal{L}_{gen}(\mathcal{X})$ denotes the family of sets of vectors accepted respectively generated by the register machines in the family $\mathcal{X}$. We will use the same notations to denote the sets of languages accepted respectively generated by any other computing device M or any other family of computing devices $\mathcal{X}$. In case the operating mode is fixed by the definition of the device (e.g., vector addition systems always generate), we omit the corresponding subscript.

We use the notation RM to refer to the family of register machines defined as above. It is folklore (e.g., see [13]) that $\mathcal{L}_{acc}(RM) = PsRE$. Similarly, register machines generate any recursively enumerable set of vectors of natural vectors, i.e., $\mathcal{L}_{gen}(RM) = PsRE$.

2.2.1. Blind and Partially Blind Machines

Several papers consider weaker kinds of register machines: blind and partially blind register machines, for example, see [2, 5, 7].

In *partially blind* register machines, the SUB instruction has the form $p : (SUB(r), q)$: if the register r is not empty, it is decremented and the register machine moves to state q, otherwise the machine crashes—the computation stops in a non-halting configuration, yielding no result. In *blind* register machines, the registers are allowed to contain negative values, meaning that the decrement instruction always succeeds. However, valid computations of a blind machine are required to have 0 in all non-output registers in halting configurations. The definitions of blind and partially blind machines may vary from source to source: notably some sources define blind register machines as partially blind, but without the zero check at the end [5].

2.3. Vector Addition Systems (VAS)

A *vector addition system* (VAS) of dimension $n \in \mathbb{N}$ is defined to be the pair $(\mathbf{w}_0, W)$, where $\mathbf{w}_0 \in \mathbb{N}^n$ is the start vector, and W is a finite set of vectors from $\mathbb{Z}^n$, called addition vectors. An addition vector $\mathbf{w} \in W$ is said to be applicable to a vector $\mathbf{x} \in \mathbb{N}^n$ if $\mathbf{x} + \mathbf{w} \in \mathbb{N}^n$, i.e., if all the components of the vector $\mathbf{x} + \mathbf{w}$ are non-negative. A VAS evolves from the start vector $\mathbf{w}_0$ by sequentially adding applicable addition vectors from W.

A *vector addition system with states* (VASS) is a VAS equipped with a finite state control. Essentially, state labels are assigned to addition vectors and a graph of states is given which defines the possible sequences of application of addition vectors.

An extended model lifting the restriction that the valid vectors must have non-negative components has recently been defined in [8] and studied in [3]: An *integer vector addition system* ($\mathbb{Z}$-VAS) of dimension $n \in \mathbb{N}$ is the pair $(\mathbf{w}_0, W)$, where $\mathbf{w}_0 \in \mathbb{Z}^n$ is the start vector and $W \subseteq \mathbb{Z}^n$ is finite set of addition vectors. A $\mathbb{Z}$-VAS evolves from $\mathbf{w}_0$ by sequentially applying the addition vectors from W. The set of vectors generated by a $\mathbb{Z}$-VAS is defined to be the set of reachable vectors.

An *integer vector addition system with states* ($\mathbb{Z}$-VASS) is a $\mathbb{Z}$-VAS equipped with a state control and is defined as a tuple $(\mathbf{w}_0, Q, q_0, q_h, p, \delta)$, where $\mathbf{w}_0 \in \mathbb{Z}^n$ is the start vector, Q is a finite set of state labels, $q_0 \in Q$ is the starting state, $q_h \in Q$ is the halting state, $p : Q \setminus \{q_h\} \to \mathbb{Z}^n$ is a function assigning a vector to every state from $Q \setminus \{q_h\}$, and $\delta : Q \to 2^Q$ is a state transition function assigning to each state the set of possible successor states. A $\mathbb{Z}$-VASS starts in $\mathbf{w}_0$ and in state q_0, applies the addition vector $p(q_0)$, and non-deterministically moves into one of the states from $\delta(q_0)$. This process is iteratively repeated, until the halting state q_h is reached. The vector language generated by a $\mathbb{Z}$-VASS is defined as the set of all vectors which are reachable in the halting state q_h.

It was shown in [10] that VASS are equivalent in expressive power to VAS (without states): any n-dimensional VASS can be simulated by an $(n+3)$-dimensional VAS. On the other hand, in [3, Section 6], it is proved that $\mathbb{Z}$-VASS are strictly more powerful than $\mathbb{Z}$-VAS. This is one first example showing that changing the nature of the objects on which a model of computing operates can affect its expressive power in important ways.

3. Register Machines and VAS over Groups

In this section we extend the definition of register machines to allow their registers to contain elements of arbitrary finitely presented groups.

Definition 3.1 *Let $m \in \mathbb{N}$ and take the finite family of finitely presented groups $\mathcal{G} = (G_i)_{1 \leq i \leq m}$, with $G_i = \langle B_i \mid R_i \rangle$. A* $\mathcal{G}$-register machine *(or a register machine over the family $\mathcal{G}$) is the construct $M_{\mathcal{G}} = (\mathcal{G}, B, l_0, l_h, P)$, where*

- *B is the set of labels bijectively labeling the instructions in the set P,*
- *$l_0 \in B$ is the initial label,*
- *$l_h \in B$ is the final label, and*
- *P is the set of instructions.*

The labeled instructions in P can be of the following forms:

- *$p : (ADD(r, b), T)$, with $p \in B \backslash \{l_h\}$, $T \subseteq B$, $1 \leq r \leq m$, $b \in B_r$.*
  Add the generator b of the group $G_r = \langle B_r \mid R_r \rangle$ to the current contents of the register r, then non-deterministically jump to one of the instructions in T.
- *$l_h : HALT$.*
  Stop the execution of the register machine.

As for conventional register machines, we consider $\mathcal{G}$-register machines as accepting and generating mechanisms. In particular, $k \leq m$ registers are designated as input registers in the accepting case and as output registers in the generating case, respectively, i.e., the register machines accept respectively generate vectors of the form $(g_1, \ldots, g_k)$, where $g_j \in G_j$, $1 \leq j \leq k$.

We observe that the ADD-instructions now allow a non-deterministic choice between an arbitrary number of target states. Moreover, no SUB-instructions are defined, as subtracting a generator b corresponds to add its inverse b^{-1}. On the other hand, there is no check for zero in these ADD-instructions.

Given a finite family of finitely generated computable groups $\mathcal{G}$, we will use the notation $\mathcal{G}$-RM to refer to the family of $\mathcal{G}$-register machines. We also use the notation $*$-$RM = \bigcup_{\mathcal{G}} \mathcal{G}$-$RM$.

Even though register machines and vector addition systems are traditionally seen as quite different models and research on one often does not discuss the other one (see, for example, the classic works [11] and [4]), the connection between the two models is clearly rather strong, especially when considered in a more general setting. For example, $\mathbb{Z}$-VASS are equivalent in power to blind register machines [3]. In the present paper, we explicitly enforce this connection by defining vector addition systems over groups in terms of register machines over groups.

Definition 3.2 *Consider a finitely generated computable group $(G, \circ)$. A* vector addition system with states over G *(a G-VASS) is a tuple (g_0, M), where $g_0 \in G$ is the start element and M is a (G)-register machine (i.e., a machine with a single register over the group G) working in generating mode and whose only register is initialized with g_0.*

Definition 3.3 *Consider a finitely generated computable group $(G, \circ)$. A* vector addition system over G *(a G-VAS) is a G-VASS with the following structure on the instructions of the underlying register machine:*

- $l_0 : (ADD(1,0), B) \in P$: *the initial instruction does not modify the contents of the register, but allows non-deterministically jumping to any other instruction, including the halting instruction.*
- *all instructions labelled by* $l \in B \setminus \{l_0, l_h\}$ *have the form* $l : (ADD(0,g), B \setminus \{l_0\})$, *with* $g \in G$: *the underlying machine can jump from any non-initial instruction to any other non-initial instruction, including the halting instruction.*

Example 3.4 *Integer vector addition systems (with states), as introduced in [8] and studied in [3], are vector addition systems (with states) over the product group* $\mathbb{Z}^n = \mathbb{Z} \times \cdots \times \mathbb{Z}$. *Indeed, the elements of* $\mathbb{Z}^n$ *are* n*-vectors of integer numbers, and the state control of the* $(\mathbb{Z}^n)$*-register machine corresponds to the state control of the integer VASS. On the other hand, since the register machine associated with a VAS over* $\mathbb{Z}^n$ *can halt at any time, any vector it reaches belongs to the generated language.*

Given a finitely generated computable group G, we will use the notations G-$VASS$ and G-VAS to refer to the families of G-VASS and G-VAS, respectively. Since vector addition systems are only considered as generating devices, we will use the notations $\mathcal{L}(G\text{-}VASS)$ and $\mathcal{L}(G\text{-}VAS)$ to refer to the families of sets of elements of G generated by G-VASS and G-VAS, respectively.

3.1. Blindness, Partial Blindness, and the Zero Test

A $\mathcal{G}$-register machine as defined in the previous section is quite "blind": it has no mechanism to make the choice of the new instruction depend on the values of the registers. A classical way to introduce such a dependence is by allowing an explicit zero-test instruction.

Definition 3.5 *Let* $m \in \mathbb{N}$ *and take the finite family of finitely generated computable groups* $\mathcal{G} = (G_i)_{1 \leq i \leq m}$, *with* $G_i = \langle B_i \mid R_i \rangle$. *A* $\mathcal{G}$-register machine with zero test *is the construct* $M_{\mathcal{G}} = (\mathcal{G}, B, l_0, l_h, P)$ *such that* $M_{\mathcal{G}}$ *is a* $\mathcal{G}$*-register machine, and the set* P *is also allowed to contain instructions of the following form:*

- $p : (0TEST(r), s, z)$, *with* $p \in B \setminus \{l_h\}$, $s, z \in B$, $1 \leq r \leq m$.
  Test if the current value of register r *is equal to the neutral element of the group* G_r; *if yes, jump to instruction* z, *if not, jump to instruction* s.

For a finite family of finitely generated computable groups $\mathcal{G}$, we will use the notation $\mathcal{G}$-RM_0 to refer to the family of $\mathcal{G}$-register machines with zero test.

Allowing an explicit zero test instruction is known to strictly increase the computational power of register machines (e.g., [7]). A much weaker way of introducing a dependency between the contents of the registers and the choice of instructions is the terminal zero test.

Definition 3.6 *Let* $m \in \mathbb{N}$ *and take the finite family of finitely generated computable groups* $\mathcal{G} = (G_i)_{1 \leq i \leq m}$, *with* $G_i = \langle B_i \mid R_i \rangle$. *A* $\mathcal{G}$-register machine with a terminal zero test *(a* blind $\mathcal{G}$-register machine*) is a construct* $M_{\mathcal{G}} = (\mathcal{G}, B, l_0, l_h, P)$ *such that* $M_{\mathcal{G}}$ *is a* $\mathcal{G}$*-register machine and, in any halting configuration, all registers which have not been explicitly designated as output must contain the neutral element of the corresponding group. We use the notation* $\mathcal{G}$-BRM *to refer to the family of* $\mathcal{G}$*-register machines with a terminal zero test.*

Remark 3.7 *Using the notation* BRM *refers to the original definition of blind register machines which we take over for the general case of $\mathcal{G}$-register machines.*

The types of register machines over groups we have defined up to now do not directly generalize the classical register machines, which can be seen as defined over the monoid of natural numbers $(\mathbb{N}, +)$: addition over the natural numbers is not invertible, because negative numbers do not belong to $\mathbb{N}$. To capture this restriction, we directly draw inspiration from the definitions of VAS and conventional partially blind register machines, and define partially blind register machines over totally ordered groups.

Definition 3.8 *Let $m \in \mathbb{N}$ and take the finite family of finitely generated computable groups $\mathcal{G} = (G_i)_{1 \leq i \leq m}$, with $G_i = \langle B_i \mid R_i \rangle$. Suppose one of the groups G_j, $1 \leq j \leq m$, is totally ordered with the total order $\leq_j$. A* $\mathcal{G}$-register machine with a partially blind register j *is a construct $M_{\mathcal{G}} = (\mathcal{G}, B, l_0, l_h, P)$ such that $M_{\mathcal{G}}$ is a $\mathcal{G}$-register machine whose register j is only allowed to contain values $a_j \in G_j$ with the property $0_j \leq_j a_j$.*

Computations in $\mathcal{G}$-register machines with some partially blind registers are defined as for $\mathcal{G}$-register machines, with the additional restriction on the values of the partially blind registers.
For a finite family of finitely generated computable groups $\mathcal{G}$, we use the notation $\mathcal{G}\text{-}PB_ARM$, with $A \subseteq \{1, \ldots, m\}$, to refer to the family of $\mathcal{G}$-register machines with partially blind registers with indices from A. This supposes that the groups of $\mathcal{G}$ with indices from A are totally ordered.
When $A = \{1, \ldots, m\}$, i.e., all the registers are partially blind, we will omit the subscript A from the notations, and we will refer to the register machine itself as being *partially blind*. We use the particular notation $\mathcal{G}\text{-}PBRM$ to refer to the family of register machines with all registers blind, and with the final zero test at the end of successful computations.
Note finally that $\mathcal{G}$-register machines with all registers blind and with the zero test instruction directly generalize classic register machines.

3.2. Forbidden Regions

While $\mathcal{G}$-register machines with partially blind registers are a generalization which is rather close to conventional register machines, imposing a total order on a group is a rather strong condition: for example, it entails the absence of elements of a finite order [12], thus excluding cyclic groups from consideration. Notice, however, that the total order is essentially used to define a forbidden subset of elements. We can therefore define another generalization of conventional register machines which imposes less constraints on the group.

Definition 3.9 *Let $m \in \mathbb{N}$ and take the finite family of finitely generated computable groups $\mathcal{G} = (G_i)_{1 \leq i \leq m}$, with $G_i = \langle B_i \mid R_i \rangle$. Let $\mathcal{F} = (F_i)_{1 \leq i \leq m}$ be a family of subsets of the groups in $\mathcal{G}$: $F_i \subseteq G_i$, $1 \leq i \leq m$. A* $\mathcal{G}$-register machine with forbidden regions $\mathcal{F}$ *is a construct $M_{\mathcal{G}} = (\mathcal{G}, B, l_0, l_h, P)$ such that $M_{\mathcal{G}}$ is a $\mathcal{G}$-register machine whose register i is only allowed to contain the elements in $G_i \setminus F_i$, $1 \leq i \leq m$.*

Computations in a $\mathcal{G}$-register machines with forbidden regions work as for $\mathcal{G}$-register machines, with the additional restriction on the values of registers.

Since groups suitably abstract a large number of objects and since forbidden regions can be used to carve particular "shapes" out of a given group, multiple connections with different domains can be traced for register machines over groups and with forbidden regions.

For a finite family of finitely generated computable groups $\mathcal{G}$, we will use the notation $\mathcal{G}$-$RM_{\neg\mathcal{F}}$ to refer to the family of $\mathcal{G}$-register machines with the forbidden regions $\mathcal{F}$.

Since we define vector addition systems over groups as particular cases of register machines, the idea of forbidden regions can be easily transported to VAS.

Definition 3.10 *Consider a finitely generated computable group $(G, \circ)$ and a subset $F \subseteq G$. A* vector addition system over G (respectively, with states) with the forbidden region F *is a vector addition system (respectively, with states) whose underlying (G)-register machine belongs to (G)-$RM_{(F)}$.*

Example 3.11 *A $\mathbb{Z}^n$-VAS with the forbidden region $F = \{(x_1, \ldots, x_n) \mid \exists i : x_i < 0\}$ is an n-component vector addition system as classically defined.*

Given a finitely generated computable group G, we will use the notation G-$VASS_{\neg F}$ (respectively, G-$VAS_{\neg F}$) to refer to the family of G-VASS (respectively, G-VAS) with the forbidden region F.

4. Expressive Power of RM and VAS over Groups

In this section we will a give a series of results characterizing the power of register machines over groups with or without ingredients. We start by considering the simplest case: no ingredients and singleton group families.

4.1. Singleton Group Families

For register machines with no ingredients, there is little difference between considering non-singleton and singleton group families. In this section, we will use the notation $\mathcal{C} = (C_k)_{0 \leq k \leq n}$ to refer to an n-step computation of a $\mathcal{G}$-register machine, where C_k is a vector of elements of the groups in $\mathcal{G}$ collecting the contents of the registers at step k.

Proposition 4.1 *Consider a $\mathcal{G}$-register machine M over a non-singleton family $\mathcal{G} = (G_i)_{1 \leq i \leq m}$, $m > 1$. Then there exists a singleton family $\mathcal{G}^0 = (G)$, a family of projections $\pi = (p_i : G \to G_i)_{1 \leq i \leq m}$, and a $\mathcal{G}^0$-register machine M^0 such that, for any n-step computation $\mathcal{C}$ of M there exists an n-step computation $\mathcal{C}^0$ of M^0 with the following property:*

$$C_k[j] = p_j(C_k^0),\ 1 \leq j \leq m,$$

where $C_k^0 \in \mathcal{C}^0$, $C_k \in \mathcal{C}$, and $C_k[j]$ is the j-th element of the vector C_k.

Proof. It suffices to take the group G to be the direct product [9] of the groups in $\mathcal{G}$: $G = \prod_{i=1}^{m} G_i$. The $\mathcal{G}^0$-register machine M^0 will thus have a single register containing vectors of values of the groups in $\mathcal{G}$. Any $ADD(j, b)$ instruction of M will be represented in M^0 by an instruction $ADD(1, \mathbf{b})$, where $\mathbf{b} = (e_1, \ldots, e_{j-1}, b, e_{j+1}, \ldots, e_m)$ is a vector consisting of the neutral elements of the groups in $\mathcal{G}$, except for the j-th element. □

The converse statement is not true, because any vectors from the direct product of G can appear in the ADD instructions of M^0, thus affecting multiple components of the vector from G at once. However, unsurprisingly, any computing step of M^0 can still be simulated by M in *multiple* steps.

Proposition 4.2 *Consider the non-singleton family of groups $\mathcal{G} = (G_i)_{1\leq i\leq m}$, $m > 1$, and take the singleton family $\mathcal{G}^0 = (G)$, where G is the direct product of the groups in $\mathcal{G}$ and $\pi = (p_i : G \to G_i)_{1\leq i\leq m}$ is the corresponding family of projections. Then, for any $\mathcal{G}^0$-register machine M^0 there exists a $\mathcal{G}$-register machine M such that, for any n-step computation $\mathcal{C}^0$ of M^0, there exists an n'-step computation $\mathcal{C}$ of M, $n' > n$, with the property:*

$$C_0[j] = p_j(C_0^0) \text{ and } C_{n'}[j] = p_j(C_n^0),\ 1 \leq j \leq m,$$

where C_0 and $C_{n'}$ are the first and the last configurations of the computation $\mathcal{C}$, and C_0^0 and C_n^0 are the first and the last configurations of the computation $\mathcal{C}^0$.

Proof. [sketch] M simulates the instruction $p : (ADD(0, \mathbf{b}), T)$ of M^0 by the following sequence of instructions:

$$\begin{aligned} p_0 &: \big(ADD\big(0, p_0(\mathbf{b})\big), \{p_1\}\big), \\ p_j &: \big(ADD\big(j, p_j(\mathbf{b})\big), \{p_{j+1}\}\big), \quad 1 < j < m, \\ p_m &: \big(ADD\big(m, p_m(\mathbf{b})\big), T\big). \end{aligned}$$

This ensures that M simulates M^0 with a constant-time slowdown and proves the statement of the proposition. □

The two previous propositions imply that, in a somewhat counter-intuitive way, blind single-register machines are a little more efficient than multi-register machines, because the former may require less computational steps to achieve a given configuration than the latter. This statement, however, becomes false with the addition of some of the ingredients we considered in the previous sections. Indeed, the zero test in a single-register machine over a direct product of groups requires that all components of the combined register should be zero; it is impossible to individually test the components. Similarly, transposing the total orders on some or all of the groups of the family $\mathcal{G}$ to their direct product is not generally possible. Forbidden regions are, on the other hand, more flexible and can be directly carried over from individual groups to components of the elements of the product.

The conclusion we make from these arguments is that, when no additional ingredients are considered, the power of register machines over groups does not depend on the number of registers.

Theorem 4.3 *Consider the family of finitely presented computable groups $\mathcal{G} = (G_i)_{1\leq i\leq m}$ and a $\mathcal{G}$-register machine M. Then there exists a $\mathcal{G}^0$-register machine M^0 over the singleton family $\mathcal{G}^0 = (\prod_{i=1}^m G_i)$ such that $\mathcal{L}_X(M) = \mathcal{L}_X(M^0)$, with $X \in \{acc, gen\}$.*

4.2. Generation and Acceptance: No Ingredients

As a consequence of the definition of VASS over groups, Theorem 4.3 implies that any $\mathcal{G}$-register machine working in the generating mode can be simulated by a VASS over the direct product of the groups in $\mathcal{G}$.

Corollary 4.4 *Consider the family of finitely presented computable groups $\mathcal{G} = (G_i)_{1 \leq i \leq m}$ and a $\mathcal{G}$-register machine M. Then there exists a G-VASS A over the product $G = \prod_{i=1}^{m} G_i$ such that $\mathcal{L}_{gen}(M) = \mathcal{L}(A)$.*

The similar statement for register machines in accepting mode does not hold. In fact, an accepting register machine either accepts or rejects any contents of the input registers.

Proposition 4.5 *Consider the family of finitely generated computable groups $\mathcal{G}$, a subfamily $\mathcal{G}_{in}$ and a $\mathcal{G}$-register machine M whose input registers correspond exactly to the groups from $\mathcal{G}_{in}$. Then $\mathcal{L}_{acc}(M) \in \left\{\emptyset, \prod_{G \in \mathcal{G}_{in}} G\right\}$.*
Proof. M can accept the empty language by never reaching the halting state. Suppose now that it accepts some input vector $\mathbf{x} \in \prod_{G \in \mathcal{G}_{in}} G$. Since the state transitions of M do not depend on the values of its registers, and since no particular conditions are checked at halting, the sequence of actions applied to accept $\mathbf{x}$ can be applied to accept any other $\mathbf{x}' \in \prod_{G \in \mathcal{G}_{in}} G$, meaning that M will accept all possible vectors in $\prod_{G \in \mathcal{G}_{in}} G$. □

Theorem 4.6 *Consider the family of finitely generated computable groups $\mathcal{G}$.*
Then $\mathcal{L}_{acc}(\mathcal{G}\text{-}RM) \subseteq \mathcal{L}_{gen}(\mathcal{G}\text{-}RM)$.
Proof. According to Proposition 4.5, it suffices to show how to generate the empty language and the language of all vectors over the groups corresponding to the output registers. The empty language can be generated by never reaching the halting state. The language of all vectors can be generated by non-deterministically adding the corresponding generators and their inverses to the output registers. □

The inclusion from the previous theorem is not strict. The following example shows a case in which the generating and accepting power are equal.

Example 4.7 *Consider the singleton group $\mathbf{1}$ containing the single element e and a group family $\mathcal{G}$ containing $\mathbf{1}$. Then the languages accepted by $\mathcal{G}$-register machines with the input register containing elements from $\mathbf{1}$ is equal to the languages generated by $\mathcal{G}$-register machines with the output register containing elements from $\mathbf{1}$. Indeed, the only two possible languages which can be accepted or generated are $\emptyset$ and $\{e\}$. As discussed previously, the first language is accepted/generated by never reaching the halting state, and the second language is accepted/generating by halting immediately.*

On the other hand, generating $\mathcal{G}$-register machines are not restricted to generating all possible combinations of values of their output registers, as the following example shows.

Example 4.8 *Consider the generating $(\mathbb{Z})$-register machine M with two states and whose only non-halting state is associated with the instruction $ADD(1, 1)$ adding 1 to the contents of its only register. When the register of M is initialized to 0, M only generates the set of natural numbers $\mathbb{N}$.*

The difference in power between the accepting mode and the generating mode puts forward an asymmetry in the definition of the two semantics: in the generating mode, the registers have the "knowledge" about their initial values, whereas in the accepting mode, no information about the register contents whatsoever is available.

4.3. Generation and Acceptance: The Zero Test

In this subsection we exhibit that allowing the zero test instruction equalizes the power of the accepting and generating modes.

Lemma 4.9 *Let $m \in \mathbb{N}$ and take the finite family of finitely presented groups $\mathcal{G} = (G_i)_{1 \leq i \leq m}$, with $G_i = \langle B_i \mid R_i \rangle$. Then there exists another family of finitely presented groups G' such that $\mathcal{L}_{gen}(\mathcal{G}\text{-}RM_0) \subseteq \mathcal{L}_{acc}(\mathcal{G}'\text{-}RM_0)$.*

Proof. Let $M_{\mathcal{G}} = (\mathcal{G}, B, l_0, l_h, P)$ be a $\mathcal{G}$-register machine with zero test. We consider $M_{\mathcal{G}}$ as a generating device, where $1 \leq j \leq k$ are the output registers. We now construct a register machine with zero test $M_{\mathcal{G}'} = (\mathcal{G}', B', l'_0, l'_h, P')$ with

$$\mathcal{G}' = (G_1, \ldots G_k, G_1, \ldots G_k, G_{k+1}, \ldots G_{m+k}),$$

i.e., every output register of $M_{\mathcal{G}}$ appears in two copies, and the first copy is designated as an input register of $M_{\mathcal{G}'}$, which now becomes an accepting device with the input registers $1 \leq k \leq m$. Given any input in the input registers, $\mathcal{G}'$ simulates $M_{\mathcal{G}}$ in the registers $k+1, \ldots, m+k$ representing the registers $1, \ldots, m$ using the instructions in P' with each register j in an instruction of P replaced by the corresponding register $k+j$ in the instructions of P'. With $M_{\mathcal{G}}$ reaching l_h, also $M_{\mathcal{G}'}$ reaches l_h. After that, in a final procedure, $\mathcal{G}'$ checks if the contents of register j equals the contents of register $j+k$ for every $1 \leq j \leq k$. In the success case, $\mathcal{G}'$ enters the final label l'_h.

For $j = 1, \ldots, k$, starting with p_1, sequences of instructions
$p_j : (0TEST(j), \hat{p}_j, p'_j)$,
$p'_j : (0TEST(k+j), p'_j, p_{j+1})$,
$\hat{p}_j : (ADD(j, -b), \{\bar{p}_j\})$,
$\bar{p}_j : (0TEST(j+r), \tilde{p}_j, \bar{p}_j)$, and
$\tilde{p}_j : (ADD(j+k, -b), \{p_j\})$
simultaneously decrement related registers j and $j+k$, $1 \leq j \leq k$, down to zero. In this construction, we define an instance of the rule $\hat{p}_j$ and an instance of the rule $\tilde{p}_j$ for every generator b of the group G_j, which allows testing registers j and $j+k$ for equality independently of the number of generators of the corresponding (finitely generated) group. In the success case, i.e., if both have been checked to be equal, the procedure continues with the next pair of registers. At the end, in the success case, we take $p_{k+1} = l'_h$. In the failure case, an infinite loop is entered. We leave the remaining details of the construction to the interested reader. We conclude that the set generated by $M_{\mathcal{G}}$ equals the set accepted by $M_{\mathcal{G}'}$. □

Lemma 4.10 *Let $m \in \mathbb{N}$ and take the finite family of finitely presented groups $\mathcal{G} = (G_i)_{1 \leq i \leq m}$, with $G_i = \langle B_i \mid R_i \rangle$. Then there exists another family of finitely presented groups G' such that $\mathcal{L}_{acc}(\mathcal{G}\text{-}RM_0) \subseteq \mathcal{L}_{gen}(\mathcal{G}'\text{-}RM_0)$.*

Proof. We now start with an accepting $\mathcal{G}$-register machine with zero test $M_{\mathcal{G}} = (\mathcal{G}, B, l_0, l_h, P)$ and construct a generating register machine with zero test $M_{\mathcal{G}'} = (\mathcal{G}', B', l'_0, l'_h, P')$, again using a similar construction of additional registers as in the proof of Lemma 4.9. $M_{\mathcal{G}'}$ randomly generates two copies of the output in registers i and $i+k$, $1 \leq i \leq k$. Then $M_{\mathcal{G}'}$ simulates an accepting computation of $M_{\mathcal{G}}$ in the registers $k+1, \ldots, m+k$ of $M_{\mathcal{G}'}$. In case l_h is reached in that way, instead of halting $M_{\mathcal{G}'}$ finally decreases all working registers $k+1, \ldots, m+k$ to zero:

For $j = k+1, \ldots, m+k$, starting with $p_{k+1} = l_h$, sequences of instructions
$p_j : (0TEST(j), \hat{p}_j, p_{j+1})$ and
$\hat{p}_j : (ADD(j, -b), \{p_j, p_j\})$
are carried out in a deterministic way, finishing with the HALT-instruction with label $l'_h = p_{m+k}$. We conclude that the set accepted by $M_{\mathcal{G}}$ equals the set generated by $M_{\mathcal{G}'}$. □

As an immediate consequence of the two preceding lemmas, we conclude that the generating and the accepting power of register machines over groups with the zero test instruction is equal.

Theorem 4.11 $\mathcal{L}_{acc}(*\text{-}RM_0) = \mathcal{L}_{gen}(*\text{-}RM_0)$.

A result similar to the one stated in Lemma 4.10 also holds true for blind register machines:

Corollary 4.12 *Let $m \in \mathbb{N}$ and take the finite family of finitely presented groups $\mathcal{G} = (G_i)_{1 \leq i \leq m}$, with $G_i = \langle B_i \mid R_i \rangle$. Then there exists another family of finitely presented groups G' such that $\mathcal{L}_{acc}(\mathcal{G}\text{-}BRM) \subseteq \mathcal{L}_{gen}(\mathcal{G}'\text{-}BRM)$.*

4.4. Vector Addition Systems over Groups

One of the classical results on vector addition systems is that, in the conventional definition of the model, adding a state control does not increase the power, because the states can be simulated using 3 additional components of vectors [10, Lemma 2.1]. This result can be naturally generalized to vector addition systems over groups with forbidden regions.

Theorem 4.13 *Consider a finitely generated computable group G, the product $G' = G \times \mathbb{Z}^3$, its subset $F = \{(g, a, b, c) \in G' \mid a < 0 \text{ or } b < 0 \text{ or } c < 0\}$, and an arbitrary G-VASS A. Then there exists a G'-VAS with the forbidden region F whose computations modulo the natural projection $p : G' \to G$ are exactly the computations of A.*

We can immediately generalize this result by replacing $\mathbb{Z}$ in the previous statement by a different group into which one can injectively (monomorphically) embed $\mathbb{Z}$.

Theorem 4.14 *Consider a finitely generated computable group G, and a totally ordered group Z such that there exists an injective homomorphism of totally ordered groups $i : \mathbb{Z} \to Z$. Take the product $G' = G \times Z^3$, its subset $F = \{(g, a, b, c) \in G' \mid a <_Z i(0) \text{ or } b <_Z i(0) \text{ or } c <_Z i(0)\}$, and an arbitrary G-VASS A. Then there exists a G'-VAS with the forbidden region F whose computations modulo the natural projection $p : G' \to G$ are exactly the computations of A.*

Remark 4.15 *The result [10, Lemma 2.1] as well as the two generalizations we give here do* not *necessarily state the equality between the families of languages generated by VAS with and without states. Indeed, the language generated by a VASS is usually taken to contain all the vectors which the VASS reaches while also being in a terminal or halting state, while the language of a VAS is often taken to be simply its reachability set. In Definition 3.3, this behavior is captured by allowing the underlying register machine of a G-VAS to halt at any time.*

A consequence of the fact that only the elements a G-VASS produces in its halting state contribute to the generated language is that a G-VASS can generate the empty language $\emptyset$ by

never reaching the halting state. On the other hand, the language of a G-VAS always includes at least the start element. This observation together with the fact that we define G-VAS as a particular case of G-VASS implies the following statement.

Proposition 4.16 *For any finitely generated computable group G, it holds that $\mathcal{L}(G\text{-}VAS) \subsetneq \mathcal{L}(G\text{-}VASS)$.*

Since this strict inclusion is rather trivial and does not reflect the intrinsic computing power of vector addition systems, in the rest of this section we will only consider G-VASS generating non-empty languages. In this setting, the increase in power due to the state control depends strongly on the underlying group. For example, $\mathbb{Z}^n\text{-}VAS \subsetneq \mathbb{Z}^n\text{-}VASS$, as shown in [3, Lemmas 6 and 7]. On the other hand, it follows trivially from Proposition 4.5 and Example 4.7 that adding states to vector addition systems over the singleton group **1** does not increase the power. We generalize these observations in the following statement.

Theorem 4.17 *If a finitely generated computable group G contains an element of order greater than 2, then $\mathcal{L}(G\text{-}VAS) \subsetneq \mathcal{L}(G\text{-}VASS) \setminus \{\emptyset\}$.*

Proof. Suppose that g is the element of G whose order is greater than 2. Suppose that there exists such a G-VAS A with the start element $g_0 \in G$ that $\mathcal{L}(A) = \{e, g\}$, where e is the neutral element of G. Then there exist two elements $h_0, h_1 \in G$ such that $g_0 h_0 = e$ and $g_0 h_1 = g$, and A executes the operations corresponding to adding h_0 to g_0 to generate e, and corresponding to adding h_1 to g_0 to generate g. Since $ord(g) > 2$, $g \neq e$, and either $h_0 \neq e$, or $h_1 \neq e$, or both. Let $h \in \{h_0, h_1\}$ such that $h \neq e$. Then, if A executes the sequence of actions corresponding to h_0, and afterwards the one corresponding to h, it will generate $g_0 h_0 h = h$. If $h \notin \{e, g\}$, then $\mathcal{L}(A) \supsetneq \{e, g\}$, which is a contradiction.

Now suppose that $h \in \{e, g\}$. By construction, $h \neq e$, so $h = g$. Suppose that A carries out the sequence of actions corresponding to h_0, then the sequence corresponding to h, and then the same sequence again. It would generate $g_0 h_0 h h = h^2 = g^2$. By hypothesis, $ord(g) > 2$, meaning that $g^2 \notin \{e, g\}$. But in this case $\mathcal{L}(A) \supsetneq \{e, g\}$, which is again a contradiction.

We conclude the proof by remarking that the language $\{e, g\}$ can be generated by a G-VASS with the starting element e and whose underlying register machine contains the single instruction $l : (ADD(1, g), \{l_h\})$. □

It follows immediately from the previous theorem that the state control already makes a difference for vector addition systems over $\mathbb{Z}_3 = \mathbb{Z}/3\mathbb{Z}$, the group of addition modulo 3. Indeed, it is impossible to construct a $\mathbb{Z}_3$-VAS generating $\{0, 1\}$: any attempt would end up putting the element 2 into the generated language.

Corollary 4.18 $\mathcal{L}(\mathbb{Z}_3\text{-}VAS) \subsetneq \mathcal{L}(\mathbb{Z}_3\text{-}VASS) \setminus \{\emptyset\}$.

On the other hand, the state control does not increase the power of vector addition systems over the two-element group $\mathbb{Z}_2 = \mathbb{Z}/2\mathbb{Z}$.

Proposition 4.19 $\mathcal{L}(\mathbb{Z}_2\text{-}VAS) = \mathcal{L}(\mathbb{Z}_2\text{-}VASS) \setminus \{\emptyset\}$.

Proof. Only the following non-empty languages over $\mathbb{Z}_2$ exist: $\{0\}$, $\{1\}$, and $\{0, 1\}$. The first two ones can be generated by a $\mathbb{Z}_2$-VAS whose underlying register is initialized to 0 or 1, respectively, and whose underlying register machine always halts immediately.

The third one is generated by a $\mathbb{Z}_2$-VAS with the start element $g_0 \in \{0, 1\}$ and with the underlying register machine containing only one instruction $l : (ADD(1, 1), \{l, l_h\})$. □

Even though Theorem 4.17 gives a sufficient criterion for the state control to strictly augment the expressive power of G-VAS, we do not claim that this criterion is necessary. Establishing a necessary and sufficient criterion is left as an open problem.

We conclude this discussion about the frontier between the power of G-VAS and G-VASS by recalling that the paper [3] considers *uniform families* of VAS, $\mathbb{Z}$-$VAS_{\cup}$, which are essentially an extension of vector addition systems allowing a finite number of start vectors instead of only one of them. In a similar fashion, we can consider uniform families of G-VAS. We denote these by G-$VAS_{\cup}$. For a finite group H, languages generated by uniform families of H-VAS turn out to be the same as those generated by H-VASS.

Proposition 4.20 *For a finite group H, $\mathcal{L}(H\text{-}VAS_{\cup}) = \mathcal{L}(H\text{-}VASS)$.*

Proof. Since H is finite, H-VASS generate finite languages. Hence, any given H-VASS A can be "simulated" by a uniform family of H-VAS without any addition elements (the underlying register machine halts immediately) and whose start elements form exactly $\mathcal{L}(A)$. □

5. Conclusion and Open Problems

In this paper we focused on generalizing the model of register machines to operate on groups instead of natural or integer numbers, thus continuing previous works aiming at generalizing related models of computing, such as vector addition systems and P systems [2, 3, 6, 8]. Generalizing register machines to groups allowed us to put forward the fundamental connection between vector addition systems and register machines.

The definitions and basic tools exhibited in this paper illustrate some of the consequences of the way in which register machines are generalized. One interesting class of problems which is still left open is the role of the nature of the underlying group in defining the frontiers of computational power. For example, Theorem 4.17 approaches one such separation between vector addition systems with and without states, but does not give a crisp borderline. On the other hand, the impact of the group being commutative is still to be explored.

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