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Size effect of electronic properties in highly arsenic-doped silicon nanowires

Tom Mauersberger[a,c,*], Imad Ibrahim[b,c], Matthias Grube[a], André Heinzig[b,c], Thomas Mikolajick[a,b,c], Walter M. Weber[a,c,d]

[a] NaMLab gGmbH, Noethnitzer Strasse 64a, Dresden 01187, Germany
[b] Chair for Nanoelectronic Materials, TU Dresden, Noethnitzer Strasse 64a, Dresden 01187, Germany
[c] Center for Advancing Electronics Dresden (CfAED), TU Dresden, Dresden 01069, Germany
[d] Institute of Solid State Electronics, TU Wien, Gusshausstrase 25, Wien 1040, Austria

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ABSTRACT

The unique electrostatic properties of semiconductor nanowires enable the realization of novel transistor types by the possibility to use surround gate architectures resembling ideal gate electrostatic control. Nevertheless one fundamental issue of semiconducting nanowire channels is the reliable control of doping to adjust the charge carrier concentration. Indeed, as dimensions scale down the surrounding media and the interfaces become more important. In this study we experimentally investigate the role of surface depletion and dielectric mismatch on the electronic charge transport of highly arsenic doped and bottom-up grown silicon nanowires. Electrical characterization of silicon nanowires (SiNWs) synthesized by Au catalyzed vapour-liquid-solid (VLS) growth and in-situ arsine (AsH_3) doping is reported for the first time. We demonstrate that high n-type doping is possible by adjusting the dopant precursor flow ratio during growth. Based on electrical measurements of individual nanowires, reproducible donor concentrations of up to 5.2×10^{19} cm^{-3} could be revealed. By measuring the electrical characteristics for individual nanowires in dependence of their radius, we show that the electrically active carrier density drastically reduces for small nanowires at radii much larger than those at which quantization or dopant surface segregation effects are expected to occur. Furthermore, enhancement of the contact transparency for small radii nanowires is demonstrated through dopant segregation upon metal silicidation. Size dependent measurement of electrical characteristics revealed improved contact resistivities as low as 1.4×10^{-11} Ωm^2.

1. Introduction

The superior electrostatic properties of surround gate nanowires are considered to be able to provide the ultimate scaling capability of conventional field effect transistors (FET) [1–3]. Their unique electronic properties make them important contenders of beyond complementary metal oxide semiconductor (CMOS) electronic switches [3]. The charge transport in those devices relies on the availability of charge carriers in the nanowire and source/drain contact regions – usually enabled by impurity doping. In bulk silicon we are somewhat used to the assumption that every dopant atom incorporated is also electrically active. For this to be true several requirements have to be fulfilled. The dopant atom has to be properly, i.e. substitutionally incorporated in the lattice, which is usually not the case after ion implantation. This makes an additional thermal treatment necessary. Furthermore, the dopant atom has to be ionized. For bulk silicon doped with standard dopants like phosphorous (P), arsenic (As) and boron (B) this is a fair approximation at room temperature with the ionization energies being only a few meV. In nanowires, due to their large surface to volume ratio, the contribution of surfaces and interfaces to surrounding dielectrics and the properties of the dielectric media itself become extremely important as they affect the dopant ionization energies [4]. The reason for the small dopant ionization energies in bulk is the shielding of the dopant's Coulomb potential by the surrounding charge carriers in the semi-infinite semiconductor. In nanowires, this shielding is reduced due to the limited volume and thus the ionization energy rises. Furthermore, it also depends on the dielectric properties of the surrounding dielectric because the dopant potential can penetrate into the nanowire's surrounding and therefore the field shielding changes. This effect was proposed theoretically [4] and experimentally verified for P-doping in SiNWs [5], indium nitride (InN) nanowires [6] and gallium nitride (GaN) nanowires [7]. Another aspect is the presence of interface states and trapped charges. Active charge carriers along the vicinity of the semiconductor/dielectric interface are expected to be trapped leading

* Corresponding author at: NaMLab gGmbH, Noethnitzer Strasse 64a, Dresden 01187, Germany.
E-mail address: tom.mauersberger@namlab.com (T. Mauersberger).

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to a depletion or accumulation zone close to the interface [8]. To investigate these effects we used doped VLS-grown nanowires as test vehicles and characterized them individually. Until now, investigations on in-situ doping of bottom-up grown SiNWs were restricted to B [9] and P [10–12]. However, the investigation of in-situ arsenic (As) doping has been missing so far despite the relevance of this donor impurity given its comparatively large solubility in bulk silicon and its low diffusivity principally enabling the capability to create ultra-sharp junctions [13]. Here, we report the first electrical characterization of in-situ As-doped VLS-grown SiNWs and study their size dependent electrical properties.

2. Experimental

Doped SiNWs were synthesized by the bottom up particle assisted vapor liquid solid (VLS)-mechanism in an industrial low pressure chemical vapor deposition (LPCVD) reactor with gold (Au) as catalyst from a nominally 1.2 nm thin sputtered film on oxide-free Si (1 0 0) substrates. Process temperature was set from 400 to 450 °C to first allow the agglomeration of the Au film into nanoparticles and the consecutive VLS-growth. Monosilane (SiH_4) was used as the precursor gas and arsine (AsH_3) as n-type dopant source. The growth time was adjusted from 20 to 30 min to yield SiNWs with lengths up to 40 µm. The diameters are homogenous along the nanowirés full length and range from 5 to 60 nm as given by the Au cluster thickness. To achieve high n-type doping, AsH_3 to SiH_4 gas flow ratios of 9×10^{-2} and 7×10^{-2} were used, resulting in active donor concentrations of 5.2×10^{19} cm^{-3} and 2.6×10^{19} cm^{-3}, respectively as determined from electrical measurements explained below. For electrical characterization, devices were fabricated by first detaching and suspending the as-grown wires in solution and posteriorly transferring them to host chips by spray dispersion. The host chips were composed of a 300 nm thick top insulating SiO_2 layer and predefined contact electrodes made from titanium/nickel (Ti/Ni). Typically, four contact leads were defined by electron beam lithography and PMMA/-(MA) double resist layer. After exposure and development, a native oxide etch in 100:1 NH_4F buffered hydrofluoric acid in HF was performed. Immediately thereafter, the samples were loaded to a sputtering tool to deposit Ti/Ni or pure Ni layers, followed by a lift-off procedure in acetone. For the first electrical characterization no annealing was performed, since intrusive silicide contacts affect the four-point measurement setup. To study dopant segregation by silicidation, Ni contacted NWs were annealed in forming gas atmosphere at 450 °C for 20 s in a rapid thermal processing furnace.

3. Results and discussion

If a nanowire is subject to electrical characterization from two electrodes, the total resistance R_T of the system can be described as

$$R_T = 2\,R_C + R_M + R_{NW} \quad (1)$$

where R_C is the contact resistance at each electrode, R_M is the total resistance of the contact metal and R_{NW} is the nanowire resistance. If the contact resistance is of the same order as the nanowire resistance a correct determination of R_{NW} is only possible by multiple terminal methods. For this study, a four-probe technique was chosen allowing the extraction of the nanowire resistivity assuming a circular nanowire cross section. As we will define later, we will call this the apparent nanowire resistivity ρ_{app} in accordance to *Björk* et al. [5]:

$$\rho_{app} = R_{NW}\frac{\pi r_{phys}^2}{L} \quad (2)$$

with r_{phys} being the physical nanowire radius and L as the probed nanowire length. Both dimensions were measured by scanning electron microscopy (SEM). This was done after electrical characterization as the excessive electron beam irradiation was found to degrade the characteristics. The thickness of the native oxide shell of around 1.8 nm as determined by transmission electron microscopy (TEM) was subtracted from all measured radii. Nanowires with radii ranging from 7 to 28 nm could be contacted and measured. Fig. 1 presents the calculated ρ_{app} versus the physical nanowire radius for two nominal doping concentrations. It tends to saturate for large diameters and exhibits a supra-linear increase as the nanowire radius decreases. This behaviour is observed clearly for both nominal doping concentrations. The nominal doping concentration N_D was obtained from the resistivity values of the thickest measured nanowires to ensure bulk properties and negligible size effects. At these diameters, resistivity saturation sets in. For these wires an empirical bulk mobility model was used to extract the doping concentration [14] as common reference works like *Sze & Ng* [15] or *Eranna* [13] don't provide values for arsenic doping in silicon. For the two corresponding dopant/precursor flow ratios studied, the nominal doping concentrations N_D of 2.6×10^{19} cm^{-3} and 5.2×10^{19} cm^{-3} were extracted. Note that for the lower doping concentration (blue symbols) even thinner nanowires than the ones provided in the figure could be measured. For nanowires with radii of 9 and 7 nm resistivities of 552 and 1130 mΩcm could be extracted, owing their I-V characteristics still being ohmic. The found size effect is similar to the one observed in semiconducting P-doped SiNWs [5] and indium nitride (InN) NWs [6] as well as in metallic Cu nano-via interconnects [16], nano-graphitic metallic carbon nanowires [17] and Cu-nanowires [18]. To explain the observed effect various phenomena are considered. Since the nanowires are single-crystalline and have smooth surfaces, we exclude the possibility of mobility degradation by scattering at grain boundaries and rough surfaces as reported in [5,6,19]. Like Björk et al. [5], we also exclude that quantum confinement takes place in the nanowires, since for silicon this is only expected for radii < 5 nm [4]. In fact, the most plausible explanations are surface depletion by either fixed charges (Q_f) or charges trapped in interface states (Q_{it}) reducing the electrically active cross section proposed by *Schmidt* [8] and donor deactivation by dielectric mismatch proposed initially by *Niquet* [4] and *Diarra* [20] and observed experimentally by *Björk* in P-doped SiNWs [5]. Nanowires grown by the VLS-method dońt have a perfect circular cross section but are typically facetted, e.g. in a hexagonal shape [21].

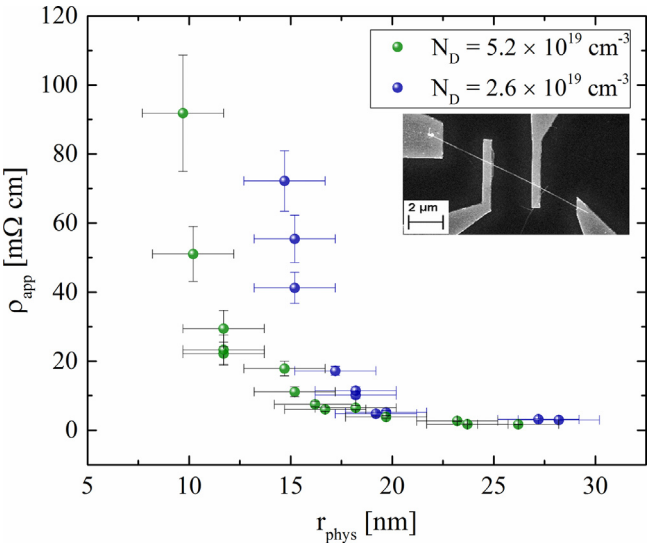

Fig. 1. Apparent nanowire resistivity ρ_{app} versus the physical nanowire radius r_{phys} for two nominal doping concentrations N_D of 2.6×10^{19} cm^{-3} (blue symbols) and 5.2×10^{19} cm^{-3} (green symbols). The apparent resistivity tends to saturate for large radii and supra-linearly increases with decreasing radius for the two nominal doping concentrations. The inset shows a scanning electron microscopy (SEM) top-view of a nanowire contacted by four titanium/nickel (Ti/Ni) electrodes. No annealing was performed after contact deposition. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

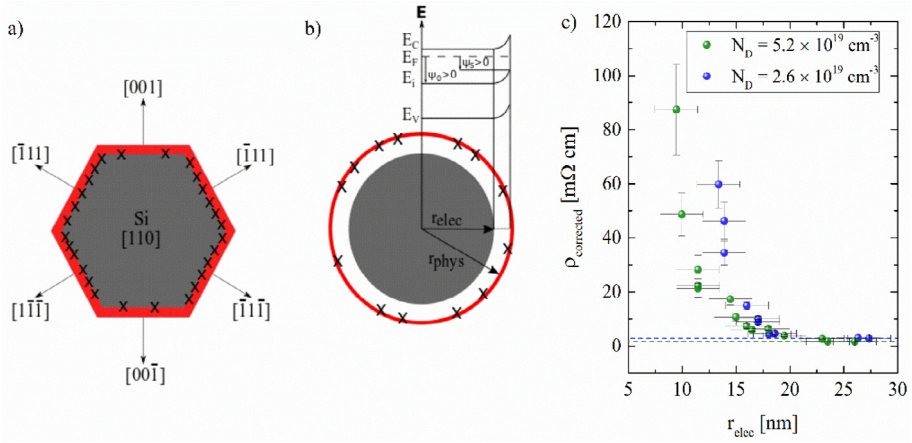

Fig. 2. a) Schematic of a [1 1 0] oriented silicon nanowires with hexagonal cross section visualizing surface orientation dependent interface trap density D_{it}. b) n-doped nanowire with thin native oxide, where a circular shape is assumed. The charged interface states with density D_{it} capture electrons at the nanowire/oxide interface, i.e. at radius r_{phys} and cause a depletion zone at the semiconductor nanowire surface leaving behind a smaller electrically active cross section with radius r_{elec} [5]. c) Corrected nanowire resistivity $\rho_{corrected}$ versus calculated electronic radius r_{elec}.

Thus, nanowires growing in (1 1 0) axis orientation, like the ones studied here, were shown to typically have four (1 1 1)- and two (1 1 0)-oriented surfaces (see Fig. 2a). This makes a considerably large part of the surface prone to charges trapped in interface states as well as fixed oxide charges as their densities typically are largest for (1 1 1)-oriented surfaces, followed by (1 1 0) surfaces as compared to ideal (1 0 0) surfaces employed in most modern MOSFETs [22]. Additionally, the nanowires are surrounded by a thin and possibly low quality native oxide, which exhibits a rather larger density of fixed oxide charges, oxide trapped charges in the dielectric and a higher level of unsaturated bonds which lead to interface states that might deplete the nanowire surface of mobile carriers by charge trapping at interface states. This means that the actual radius carrying the charge could be significantly smaller than the physical radius measured by SEM. In literature this is usually expressed in terms of a physical nanowire radius r_{phys} that is reduced to a charge carrying electronic radius r_{elec} (Fig. 2b). The interface states will capture electrons from the surface of a n-doped nanowire leading to a depletion zone visualized by the white annulus in Fig. 2b. By solving *Poisson's* equation in polar coordinates and adopting a full depletion approximation, the electronic nanowire radius can be calculated by [8]:

$$r_{elec} = \sqrt{r_{phys}^2 + \frac{2r_{phys}Q_f - 2r_{phys}q^2D_{it}\varphi_0}{q(N_D - N_A)\left(1 + \frac{r_{phys}q^2}{2\varepsilon_0\varepsilon_s}D_{it}\right)}} \quad (3)$$

where Q_f is the fixed oxide charge density, q is the elementary charge, D_{it} is the density of interface trapped charges, φ_0 is the electrostatic potential at r = 0, ε_0 and ε_s are the relative dielectric constants of vacuum and the semiconductor and finally $N_{D,A}$ is the donor or acceptor concentration. For the following discussions Q_f was set to zero, as the effect of fixed charges on the nanowires electronic properties is assumed to be rather weak compared to charges trapped in interface states [8]. For a correct determination of the nanowire resistivity the electronic radius has to be used. A popular method for determination of interface state density is C-V characterization. While for top down nanowire FETs test structures with a large amount of parallel nanowire channels can be used [23], the estimation for VLS-grown nanowires is more complex as parallel nanowires would preferably need the same size and alignment, such that little data is found in literature [24]. Due to the stochastic size distribution and corresponding preferred crystal orientation [25,26], the density of interface states is an average value over a broad range of diameters with different D_{it} levels. For further analysis a rather high D_{it} of 1×10^{13} eV^{-1} cm^{-2} was assumed since values in this range but slightly smaller have been reported by Cassé et al. [23] for silicon nanowires with round cross section near the band edges. The high level assumed here also accounts for the lack of annealing in our devices and the presence of only a thin low quality native oxide [27]. Fig. 2c) presents the measured resistivity ρ_{app} corrected for surface depletion by charges trapped in interface states, yielding the corrected resistivity $\rho_{corrected}$. From a comparison to the experimental data in Fig. 1, it can be seen that even for a very high density of interface traps, the effect of surface depletion for the two doping concentrations used in this study is very weak. To further circumvent this effect and to strongly decrease D_{it}, one could replace the native oxide by a high quality thermal oxide, followed by an anneal in forming gas-atmosphere to passivate the remaining interface states [28]. The two dashed horizontal lines show the resistivity values of the thickest nanowires as well as the resistivity if in the measured nanowires only surface depletion by charges trapped in interface states would degrade the resistivity. As the resistivity still increases for thinner nanowires, there has to be an additional effect impacting the electrical properties. This effect is most probably dopant deactivation by dielectric mismatch between the nanowire and the surrounding SiO_x shell and outer air, as the other possibilities were already excluded. Until now, it was assumed that all the dopants that are present in the nanowires are also active, i.e. they are ionized generating a free electron that can contribute to a current flowing through the nanowire. One important aspect is the screening of the dopant potential. If we consider a single donor atom in silicon, a certain energy is required to remove the outermost electron from the shell. As the extracted dopant concentrations 5.2×10^{19} cm^{-3} and 2.6×10^{19} cm^{-3} are near the *Mott transition* (N_{crit}) of arsenic doped silicon [29], one can describe this problem as an electron that is trapped in a finite quantum well, where only a certain number of bound states can exist. The more dopant atoms there are, the stronger the potential of this impurity can be screened. This means that the quantum well, where the electron is trapped gets narrower, leading to the energy of bound states to rise. Increasing the concentration of dopants even further eventually leads to a "drop out" of the energy level of the outermost bound state from the quantum well. That means that the electron in this state is no longer bound to the donor and is now free to move inside the silicon. For that to happen these donor atoms have to have a critical distance, i.e. a critical screening length allowing the interaction of dopant potentials. As the screening length is an unhandy quantity that we cannot directly influence, it is much more common for semiconductors to express it in terms of a critical doping concentration N_{crit}. From that concentration on, the dopant potentials become strongly screened and as an overall effect the ionization energy is drastically reduced. In literature this phenomena is usually described by a doping concentration dependent ionization energy [29]:

$$E_I(N_D) = \frac{E_{I,0}}{1 + \left(\frac{N_D}{N_{crit}}\right)^c} \quad (4)$$

With $E_{I,0}$ (As) = 54 meV, $N_{crit} \approx 3 \times 10^{18}$ cm^{-3} and c = 1.5. Arsenic impurities in bulk silicon with a concentration of e.g. $N_D = 10^{19}$ cm^{-3} would have an ionization energy of only 7.6 meV,

being even less than the thermal energy at room temperature. For this reason, it is safe to assume that in bulk silicon practically all dopants are ionized. For nanowires, on the contrary, the situation is different. The impurity potentials are not sufficiently screened within the nanowire anymore, but inside the surrounding medium. In practical cases, this medium is a dielectric and its properties therefore greatly influences the properties of the nanowire. *Diarra* et al. studied this problem theoretically and found that with decreasing nanowire radius, the screening reduces and the dopant ionization energies rise [20]. An expression was found that clearly states the importance of the dielectric surrounding of a nanowire with radius r:

$$E_I(r) = E_{I,0} + \frac{2}{r\varepsilon_s}\frac{\varepsilon_s - \varepsilon_{out}}{\varepsilon_s + \varepsilon_{out}} F\left(\frac{\varepsilon_s}{\varepsilon_{OUT}}\right) \quad (5)$$

where $E_{I,0}$ is the bulk ionization energy of the dopant and ε_s and ε_{out} are the relative dielectric constants of the semiconductor nanowires and its surrounding dielectric. The function F(x) was given by *Niquet* et al. [4]. The closer the dielectric constants of the semiconductor nanowire and its dielectric surrounding are, the closer is the ionization energy to the bulk case ($\varepsilon_s = \varepsilon_{out}$) and the less pronounced is the effect of increased E_I for small nanowires. To understand how this effects the resistivity of nanowires, the charge neutrality condition was used:

$$N_C \frac{2}{\sqrt{\pi}} F_{1/2}\left(\frac{E_F - E_C}{kT}\right) = \frac{N_D}{1 + g_D \exp\left(\frac{E_F - E_D}{kT}\right)} \quad (6)$$

where N_C is the effective density of states in the conduction band, $F_{1/2}(x)$ is the Fermi integral, E_F, E_C and E_D are the Fermi energy, conduction band energy and donor energy level. g_D is the degeneracy level of the conduction band, k is the *Boltzmann* constant and T is the temperature. The equation says that the concentration of free electrons n is equal to the concentration of ionized donors N_D^+, which is the case for highly doped semiconductors. The effect of increased ionization energy is a change of the donor energy level which in turn changes the concentration of ionized donors. By solving this condition graphically like proposed in [15], the radius dependent E_F, E_C and E_D were determined (Fig. 3a). For this analysis the bandgap energy was assumed to be constant with radius, which is a fair assumption for the used size of nanowires [4]. From the fermi energy the concentration of active carriers can be determined by inserting $E_F(r)$ into the left or right hand term in equation (6) (Fig. 3b). Finally it was possible to calculate the resistivity by using the fundamental relationship:

$$\rho = \frac{1}{nq\mu} \quad (7)$$

where μ is the electron mobility. In nanowires, the mobility is mainly affected by surface scattering and the crystal orientation. It has been found by simulations, that surface scattering only affects nanowires with radii smaller than 4 nm [30,31]. For nanowires with radii larger than 7 nm the electron mobility converges to the universal mobility curve for planar silicon MOSFETs. A significant influence of crystal orientation is not expected for radii larger than 6 nm [32]. Furthermore, there is no conclusive study about charge carrier mobility in silicon nanowires which clearly states if its larger or smaller than in bulk silicon [24]. Therefore, it was assumed that the only factor influencing the mobility is the radius dependent charge carrier concentration given by the donor deactivation effect. The resulting resistivity according to the dielectric mismatch effect is plotted in Fig. 3c) together with the data of Fig. 2 versus the electronic radius to account for surface depletion by charges trapped in interface states. The general trend of the model seems to fit qualitatively well to the experimental data, but the sudden increase of resistivity for small nanowires starts already for thicker nanowires than one would expect by just considering surface depletion and dielectric mismatch – an observation which is different than the reports on P doped SiNWs by *Björk* [5]. The found shift could be due to several effects: 1) the electron mobility in nanowires could be seriously degraded especially for the thinnest nanowires compared to bulk. 2) As only little is known about the dopant incorporation mechanism during VLS-growth, especially for As-doping, the number of incorporated atoms could be radius-dependent. 3) The arsenic dopant atoms could segregate at the interface to the native oxide. This was already shown to happen by simulation and experiments for silicon and germanium nanowires doped with boron and phosphorous [33–36], however it is unknown for arsenic.

Nanowires contacted by pure Ni leads not necessarily exhibited ohmic characteristics. For radii smaller than 15 nm the characteristics became supralinear, thus it was not possible anymore to correctly determine the resistivity. Note that those nanowires were not included in Figs. 1–3. It remains unclear whether the reduced contact area und thus the contact resistance or a possible lowering in the effective donor concentration and involved Schottky junctions are responsible for this effect. The pure Ni electrodes on Si nanowires open up the possibility to use silicidation for improving the contact properties. Silicides have a low resistivity and can withstand high temperatures [37], which made them attractive for industrial semiconductor devices. Especially Ti-,

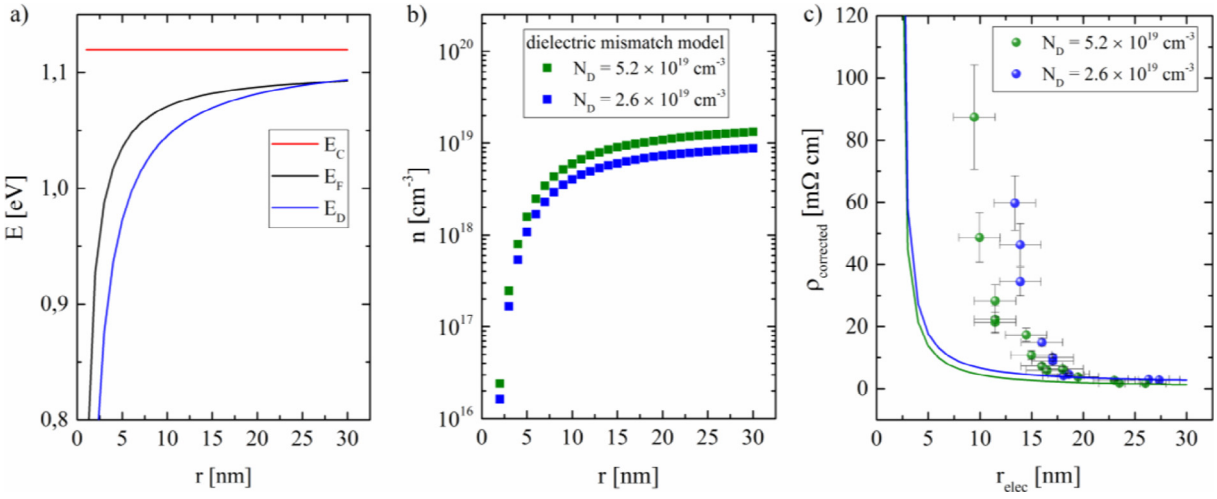

Fig. 3. a) Calculated Fermi energy E_F, conduction band energy E_C and donor energy level E_D versus nanowire radius r according to the dielectric mismatch model for nanowires with a doping concentration $N_D = 2.6 \times 10^{19}$ cm^{-3}. b) Concentration of free electrons n calculated from the radius-dependent fermi energy E_F for the two nominal doping concentrations. c) Corrected nanowire resistivity $\rho_{corrected}$ versus electronic radius r_{elec}. The solid lines represent the resistivity calculated from the dielectric mismatch model for both nominal doping concentrations and show that additional effects are required to match the observed behaviour.

Co-, W-, Pt- and currently Ni-silicides are commonly used in MOSFETs for contacting of source-/drain-regions and the gate electrodes. In the classical MOSFET technology this is achieved by depositing the corresponding metal on top of the contacts. A thermal process will then selectively silicidize desired Si-regions. In nanowires, a silicidized contact can be achieved by thermally activated intruding of metal silicide in the nanowire creating a longitudinal heterostructure [19]. This shifts the active metal–semiconductor junction inside the nanowire and effectively reduces the contact area to the cross section area of the silicon/silicide interface. The created interface was shown to be atomically sharp in other experiments involving nominally intrinsic SiNWs [38]. In this contact geometry the effect of Fermi-level-pinning at the interface is reduced and the Schottky barrier should only be given by the nominal difference of metal work function and semiconductor electron or hole affinity [39]. As the nanowires are still surrounded by a low quality native oxide, they should still be prone to surface depletion by charges trapped in interface states and donor deactivation by dielectric mismatch. After silicidation, the nanowires were measured again and the resistivity data was analyzed using the same procedure as explained before to determine the corrected resistivity and the dielectric mismatch model. It must be noted, that in this case and different to our device setup described above the contacts are now intrusive throughout the full nanowire diameter which means that the forced current from the outer electrodes is injected through six consecutive Schottky junctions. Nevertheless, the current voltage characteristics of the same device became ohmic upon silicidation. The results are plotted in Fig. 4. The resistivities of thin nanowires improved substantially, e.g. a nanowire with a physical radius of 15 nm contacted by Ti/Ni had resistivities of up to 70 mΩcm whereas the resistivity of nanowires with silicidized contacts of the same radius decreased to 4 mΩcm. With silicidized contacts, the dielectric mismatch model captures the majority of the experimental data quite well. The inset of Fig. 4 shows an SEM top view of a silicidized nanowire with well distinguishable nickel silicide phases. The nickel-rich silicide attributed to the section adjacent to the nickel contact lead has a larger lattice constant than silicon, leading to a volume expansion of approximately 30% [19]. The leading phase towards the pristine Si nanowire is assumed to be cubic $NiSi_2$ with CaF_2 structure with a comparable lattice constant to that of silicon in accordance with [19,40]. To further investigate the contact properties, the contact resistivity was studied next. It can be calculated from the absolute contact resistance R_C and the contact area A_C:

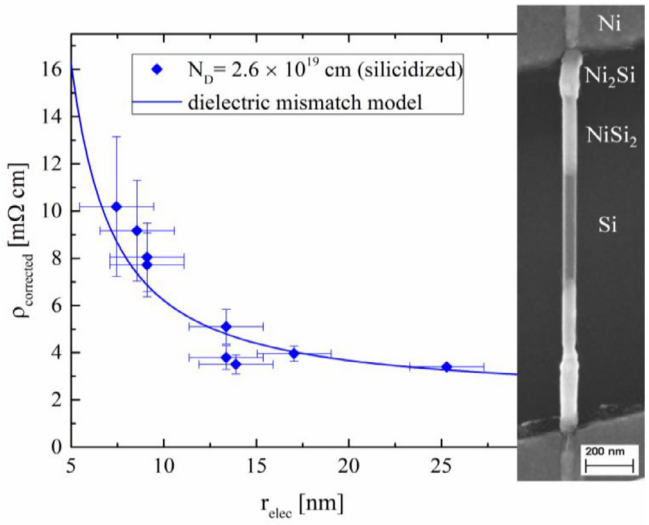

Fig. 4. Corrected nanowire resistivity $\rho_{corrected}$ of silicidized nanowires. The solid line shows the dielectric mismatch model. The right hand image show an SEM top view of a silicidized nanowire with corresponding nickel silicide phases.

$$\rho_C = R_C \cdot A_C \tag{8}$$

The contact resistance can be determined from a measurement of the total device resistance using equation (1). Usually, determining the contact area is not trivial as can be seen in Fig. 1 or Fig. 5 a) for nanowires contacted by a thin metal lead on top of it. Current transport might not take place uniformly in this contact, rather it will occur near the edges of certain geometries. However, *Mohney* et al. developed a transmission line model to calculate contact resistivities for nanowires contacted like that by assuming that 75% of the nanowires surface is covered by evaporated contact leads [41]. For intruded silicide contacts the contact area is an ellipsoid or circle spanned by the nanowire radius (see Fig. 5b). This contact geometry eliminates the use of a transmission line model as the current transport is expected to take place uniformly across the $Si/NiSi_2$ interface inside the nanowire. The calculated contact resistivity versus nanowire radius is shown in Fig. 6a). With increasing radius the contact resistivity exponentially decreases down to $(1.4 \pm 0.2) \times 10^{-11}$ Ωm^2 for the thickest measured nanowire with a radius of around 26 nm. This is close to the lowest measured contact resisitivity to a silicon nanowire so far of 1.2×10^{-11} Ωm^2, obtained for P-doped VLS-grown NWs with significantly larger nominal doping concentration of $N_D = 9 \times 10^{19}$ cm^{-3} [11]. There, evaporated Ti/Au contacts were used and ρ_C was determined by the transmission line model by *Mohney* et al [41]. The reason for the extremely low contact resistivities in our nanowires is most probably dopant segregation. For planar silicon it was shown that upon silicidation the dopant atoms tend to accumulate at the intruding interface between silicon and the respective silicide due to the fact that theýre not or only hardly soluble in the silicide [42]. This means that a thin interlayer with a high amount of dopant atoms will form at the interface (see Fig. 5b). The Schottky barrier becomes thinner, allowing tunneling for electrons with energies lying closer to the fermi energy [43]. It is not expected, that the atoms are substitutionally incorporated within the silicon lattice at the used silicidation temperatures. However, it has been shown that dopants show an important effect on charge transport at the contact interface. Effectively reducing the Schottky barrier (SB) height, dopant segregation makes the metal semiconductor junction more transparent for charge carriers [44]. For this reason segregated dopants were originally proposed to reduce the SB height in SB MOSFETs, where the ON-current is dominated by the barrier [45]. Dopant segregation in nanowires is a versatile instrument to create sharp interfaces, since other methods like ion implantation or switching gases during VLS-growth are difficult in such geometries. Hereby a method for determining the effective SB height of intruded segregated Si/silicide junctions is proposed, which makes use of the size effect of active doping concentration discussed before. By determining the contact resistivity for individual nanowires of different radii, one can cover a large range of apparent doping concentrations albeit only one single nominal doping concentration is present. By plotting the natural logarithm of the contact resistivity versus the inverse of the square root of the apparent doping concentration $N_{D,app}$ one can clearly distinguish at least two different regimes (Fig. 6b). For very high doping concentrations, the transport mechanism across the junction is mainly field emission (FE)/tunneling. In this regime, the contact resistivity is determined by the number of free charge carriers in the semiconductor and a huge sensitivity on the doping concentration is expected [46]. In this regime the contact resistivity can be described in the following form:

$$\rho_{C,FE} \sim \exp\left(\frac{\Phi_{Bn}}{\sqrt{N_D}}\right) \tag{9}$$

Here, Φ_{Bn} denotes the effective Schottky barrier height for electrons and N_D is the electrically active doping concentration. This concentration is given by the respective resistivity ρ_{app} of the individual nanowires and an empirical bulk mobility model was used to determine the apparent doping concentration $N_{D,app}$ [14]. From a linear fit to the plot to the experimental data for the highest doping concentrations, one can

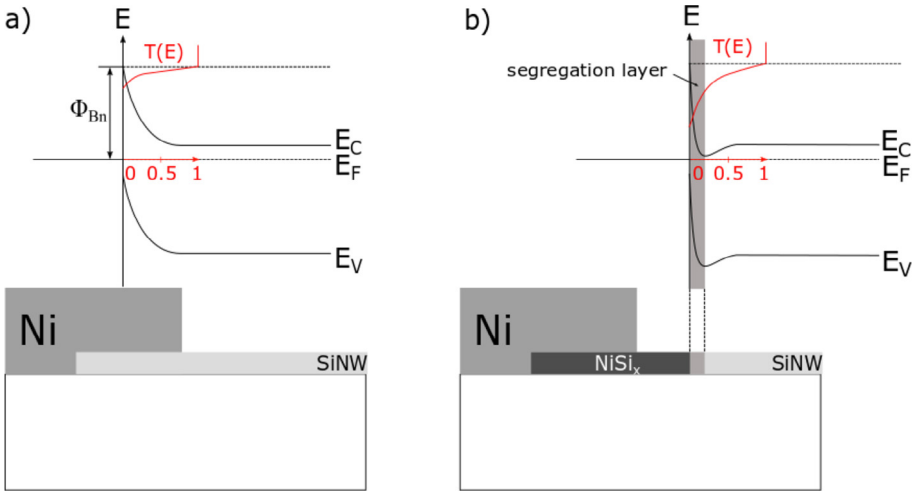

Fig. 5. Comparison of injection efficiency for conventional Schottky junctions and dopant segregated Schottky junctions after silicidation a) Schematic of a Ni-contacted n-doped silicon nanowire and the corresponding schematic band diagram of the Ni-SiNW Schottky junction. Fermi-level alignment leads to band bending at the interface. In the ideal case the Schottky barrier Φ_{Bn} is given by the difference in metal work function and electron affinity of the n-doped semiconductor. Red lines and scale display the energy-dependent tunnelling probability T(E). In this case electrons contributing to the tunnel current have energies located slightly below the barrier maximum. b) The same nanowire after silicidation. The Schottky $NiSi_x$/SiNW junction intruded within the nanowire. This creates a thin interlayer with a high concentration of dopant atoms (denoted as segregation layer). The Schottky barrier becomes thinner and the decrease of T(E) is less pronounced for lower energies. Electrons with energies closer to the Fermi energy E_F contribute to the current and tunnelling dominates the transport. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

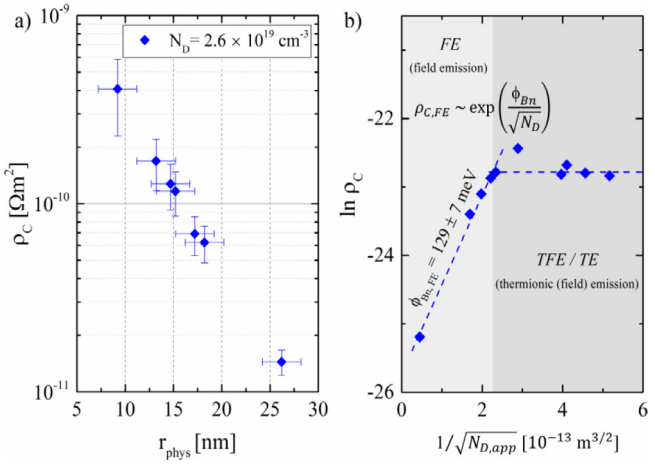

Fig. 6. a) Contact resistivity ρ_C of the nanowire/silicide contact for a nominal doping concentration of 2.6×10^{19} cm^{-3} vs. physical nanowire radius r_{phys}. b) Natural logarithm of contact resistivity ρ_C vs. inverse square root of apparent doping concentration $N_{D,app}$. The Schottky barrier height Φ_{Bn} can be extracted from the slope in the field emission (FE) regime.

extract the effective Schottky barrier height. For the parameters used here, this method yields a SB height of 129 ± 7 meV. This value is close to already reported values around 100 meV for As segregated $CoSi_2$/bulk-Si junctions [45]. From a certain apparent doping concentration on, ρ_C starts to saturate and will stay constant for the measured range of doping concentrations. This is a hint for a change in transport mechanism, probably from field emission to thermionic emission. In between a mixture of both transport mechanisms will take place [46].

4. Conclusions

Electrical characterization of bottom-up VLS-grown in-situ As-doped SiNWs was shown for the first time. 4-point measurements of individual nanowires of different diameters and different dopant precursor flow ratios revealed doping is possible by changing the gas flows during growth. An intricate size effect of nanowire resistivity was found, mainly attributed to surface depletion by charges trapped in interface states and donor deactivation by dielectric mismatch. Ni-contacted NWs were silicidized, leading to substantial improvements of resistivity and contact properties owing to the special contact geometry and an effect called dopant segregation. By measuring the contact resistivity of individual silicidized nanowires of different diameters, a large range of active doping concentrations could be covered. By plotting the contact resistivity versus the electrically active doping concentration different transport mechanisms across the metal semiconductor junction could be revealed. An effective Schottky barrier height of approximately 130 meV was extracted, which supports the assumption of dopant segregation upon silicidation. The found results have important implications for scaled devices. For field effect transistors, regions not covered by the gate need to be doped very highly to account for donor deactivation. Similarly, changing the dielectric not only changes the gate capacitance, but also the number of active charge carriers in the channel. For nanowires, intruded silicide contacts represent the optimal metal semiconductor junction due to the unique contact geometry and the dopant segregation effect, both contributing to substantially improved conductivity and contact properties.

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