Inherent Charge-Sharing-Free Dynamic Logic Gates Employing Transistors with Multiple Independent Inputs

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Abstract — Charge sharing poses a fundamental problem in the design of dynamic logic gates, which is nearly as old as digital circuit design itself. Although, many solutions are known, up to now most of them add additional complexity to a given circuit and require careful optimization of device sizes. Here we propose a simple CMOS-technology compatible transistor level solution to the charge sharing problem, employing a new class of field effect transistors with multiple independent gates (MIGFETs). Based on mixed-mode simulations in a coordinated device-circuit co-design framework, we show that their underlying device physics provides an inherent suppression of the charge sharing effect. Circuit layouts and design examples are discussed, which elucidate the fundamental differences in circuit topology to classical CMOS designs. For example it is shown that dynamic gates from MIGFET scale much better with stack height of long serial networks, leading to an increased circuit performance, while also providing higher signal stability.

Index Terms — dynamic logic gates; charge sharing, domino logic; reconfigurable transistor; Schottky transistors; multigate

I. INTRODUCTION

DYNAMIC logic is a design methodology which has been widely used in modern microprocessors, due to its benefits in terms of area, performance and power consumption over other logic families, such as static logic, pseudo-NMOS logic and complementary pass transistor logic (CPL) [1]. In order to build any $N$-input function only $N + 2$ transistors are needed in dynamic logic, while $2 \cdot N$ transistors are needed in complementary static CMOS design [2]. While both static and dynamic logic can eliminate static power dissipation by design, dynamic logic gates can be up to twice as fast as their static counterparts. This is especially important for logic functions with many inputs, such as 4-NAND or 4-NOR logic gates.

On the other hand, dynamic logic gates suffer from a number of reliability problems and circuit design constraints [3], [4]. First of all, dynamic gates facilitate a two-step operation scheme, which is controlled by an external clock. During a pre-charge phase, the output of a gate is temporarily charged. Then, during evaluation the capacitance is discharged depending on the conditions of logic inputs of the gate. As the evaluation step is non-reversible dynamic gates require monotonically rising inputs during evaluation. Conversely, dynamic gates produce monotonically falling outputs. As a result, it is forbidden for one dynamic gate to drive another one. This typically inflicts issues with clock synchronization and timing. A typical solution are domino circuits, where alternating dynamic and static logic gates are cascaded. Further stability problems can be caused if the volatile charge is lost during the evaluation process either by leakage across the channel or through the reverse-biased diode of the diffusion area [5].

Another very specific issue to dynamic gates is the so-called charge sharing problem. This is a signal integrity phenomenon where the charge stored at the output node is redistributed during the pre-charge phase towards the internal

Figure 1. The charge sharing problem in a dynamic logic gate. (a) Circuit schematic of a footed dynamic 2-NAND logic gate. (b) Schematic waveforms during operation. While the clock singal (CLK) is 0, the output node $C_L$ is pre-charged. During, evaluation ($V_{CLK}=1$) the output node is discharged, if A and B is at 1 (dashed red lines). The output node will stay charged, if at least A or B is at 0 and the PDN is off (solid lines). If signal A is switched during evaluation charge will be redistributed from the output node $C_L$ to the internal node $C_{a,i}$. This charge sharing effect can disturb the readout of the logic gate.
junction capacitances of the network which is in the evaluation phase [6]. Similar to charge leakage, charge sharing can degrade the output voltage level and thus cause an erroneous output value. As device geometries are scaled down, leakage currents and charge sharing become increasingly critical problems, especially in full-custom circuit designs [7]. As a result dynamic logic styles have become unpopular in modern microelectronics, because the signal integrity of the circuit is at risk, especially when the design does not account for possible charge sharing.

In this paper it will be demonstrated how a new class of transistors, the so called multiple independent gate field effect transistors (MIGFETs), can be employed to eliminate the charge sharing problem without the need for any additional circuitry. This paper thereby is organized as follows. In section II the charge sharing problem as well as some known circuit-level solutions will be introduced in detail. In section III multiple independent gate field effect transistors (MIGFETs) based on gated nanoscale Schottky junctions are reviewed. Demonstrator devices utilizing fully-depleted silicon-on-insulator (FD-SOI) channels are discussed. In section IV, it will be explained how the underlying operation principle of these devices can be used to eliminate the charge sharing issue at the device level. A discussion on the circuit level performance of those gates as well as a design example will be given in V. Finally, a conclusion is drawn in section VI.

II. THE CHARGE SHARING PROBLEM

Figure 1 illustrates the operation principle of a simple dynamic 2-NAND logic gate including the charge sharing problem. During the pre-charge phase, the clock-controlled pull up network (PUN) is opened and the output node \( C_L \) is charged. During the evaluation phase the PUN is closed and \( C_L \) will either be discharged, if the inputs \( A \) and \( B \) are both at high level or it will retain its value if one of the input signals is low. The charge sharing effect only becomes relevant, when the last stage (here input A) of the pull down network (PDN) alters its state during the evaluation phase. In this case, charge is redistributed between the output to the internal node \( C_{a,i} \). The corresponding voltage change at the output can be estimated by:

\[
\frac{\partial V_{\text{OUT}}}{\partial t} \approx \frac{C_{a,i}}{C_L} (V_{DD} - V_{TH}) \tag{1}
\]

The effect becomes severe, if the induced drop reaches below the threshold voltage of the transistor in the evaluation network (typically a p-type device in the PUN as drawn in Fig. 1). As a rule of thumb, the capacitance of the internal node \( C_{a,i} \) has to be smaller than \( 1/5 \) of the output capacitance \( C_L \) to be uncritical. However, if the number of series FETs in the PDN increases, i.e. the number of inputs increases, charge sharing becomes a more severe problem, because the number of internal capacitances that potentially can share charge increases. Therefore, charge sharing is one of the factors that limit the stack height of dynamic logic gates.

As dynamic logic designs have been a major part of modern microprocessors, there are several known solutions that can be used to minimize charge sharing as well as charge leakage with the help of additional circuitry as shown in Figure 2. Using so called bleeder (Fig. 2a) or keeper (Fig. 2b) circuits, the charge lost at the output is restored via a weak transistor in the case of a switching event, but still deliver sufficient current to suppress charge sharing. Another option (Fig. 2c) is to pre-charge the internal node \( C_{a,i} \) so that it will have the same potential as the output node [4]. Unfortunately, all these solutions not only require additional transistors, but also add an additional source for power dissipation to the system. Thus, a solution without the need for additional circuitry would be desirable. Here it will be shown that such a solution can be provided by MIGFETs.

III. SCHOTTKY BARRIER BASED TRANSISTORS WITH MULTIPLE INDEPENDENT GATES

MIGFETs are a relatively novel class of emerging devices that are based on gated low-dimensional semiconductor Schottky junctions. They are extensions of the more-well known polarity-controllable or reconfigurable field effect transistors (RFETs) and thus are able to offer multiple operation states [10]–[13]. Exploiting the plurality of gate electrodes REFTs merge unipolar p- and n-type conduction into a single device. The desired device operation type is programmed by an electric signal. Different from conventional complementary metal oxide semiconductor circuits, no doping is generally required. All materials and process steps needed are
Figure 6. Simulated transfer characteristics of scaled MIGFETs with 4-gates and 128 nm channel length used for circuit simulations in Fig. 4(e-f). Open symbols relate to CG1 aligned at a Schottky contact. Full symbols relate to CG2/3 in the center of the channel. Diamonds correspond to a symmetric device, which can be programmed to either p-type or n-type behavior of similar performance. Triangles correspond to a MIGFET tuned towards improved n-functionality. Circles correspond to a MIGFET with improved p-functionality. A nanowire device demonstrating this functionality is shown in Figure 3. The channel was formed on a nanowire etched from a SOI substrate. After gate oxide formation by rapid thermal annealing, sharp NiSi$_2$ source and drain contacts were formed. The program gate (PG), which is aligned atop the drain sided Schottky junction, thereby blocks the undesired carrier type. In addition three independent control gates (CG) are used for operation. Although the devices exhibit a reduced subthreshold slope and a lower V$_{TH}$ when steered at a control gate aligned in the middle of the channel (CG2, CG3), the on-current is the same for all three inputs as demonstrated in the

Figure 4. Circuit schematics, layouts and transient simulations for dynamic 2-NAND gate variants. (a) simple footed CMOS realization, (b) corresponding circuit layout, (c) circuit behavior in the charge sharing case and (d) circuit behavior with an open pull down network. (e) Realization using a single MIGFET with four independent gates, (f) corresponding circuit layout, (g) circuit behavior in the charge sharing case and (h) circuit behavior with an open pull down network. Switching speed increases with a reduced effective contact work function WF$_{C,eff}$ of source and drain, corresponding to the device characteristics in Fig. 6.
measured subthreshold characteristics (Figure 3b). More detailed insights into the device operation principle are given in Ref. [11].

IV. ELIMINATING CHARGE SHARING AT THE DEVICE LEVEL

Analysis of the charge sharing event was carried out by mixed-mode TCAD simulations using a similar MIGFET layout with scaled geometries that is patternable in a technology with 24 nm minimal feature size (128 nm channel lengths, 4 individual gates of 24 nm lengths each, 6 nm silicon channel width, 5.6 nm HfO$_2$ dielectric, corresponding to 1 nm EOT and TaN electrodes with 4.62 eV work function.)

Typically, a NiSi$_2$ Schottky contact having a work function of 4.71 eV to provide near midgap band alignment is used to realize symmetric p- and n-functionality [22]. More details about the simulation setup and considered transport models can be found in Ref. [16], [21]. The data is compared to mixed-mode simulations of a CMOS reference design in 22 nm FD-SOI technology [23].

Circuit schematics, layouts and mixed-mode simulation results of dynamic 2-NAND gates in both technologies are shown in Figure 4. Looking at the CMOS data first, the drain sided junction region is charged during the charge sharing event, which is in accordance with the theory explained in section II. As a result, the output capacitance $C_L$ is partially discharged and so that the electrical potential of the intermediate node $a$ is and the output equalize (Fig. 4(c)). This effect can be prevented if the PDN is replaced by a single MIGFET with four individual gates. Here, both inputs A and B are connected to the channel gates CG2 and CG3 while the clock signal is connected to the CG1 controlling the source sided Schottky junction. The program gate is used to set the polarity of the MIGFET to an n-type operation and block parasitic charge leakage via the drain sided Schottky barrier. In addition, the unique multi-gate device layout inherently suppresses charge sharing. As opposed to a normal CMOS design, the ungated area between each of the gates is a part of the channel and both control gates CG2 and CG3 exhibit a strong coupling to the ungated area between them. Consequently, in MIGFETs there is no internal junction depletion region to be charged. As the device operation is purely diffusion driven, no charge is stored within the channel before the charge sharing event. The strong local electric field induced by the blocking signal B additionally counteracts any attempt of charge redistribution from the source side (Figure 5). As a result, negligible charge is lost at the output $C_L$ during a potential charge sharing event, as shown in Figure 4(g).

Comparing the layouts of both CMOS and MIGFET realization it is obvious that the MIGFET version requires slightly more area to accommodate the additional gate needed to set the polarity. However, this gate can be conveniently hard-wired to the supply lines as shown in Figure 4(f).

Overall, the space needed for the MIGFET solution will therefore be lower than for conventional circuit based solutions requiring substantial overhead as discussed earlier in section II.

V. DISCUSSION ON PERFORMANCE

A. Device Level Performance Enhancements

The main application for dynamic logic gates are critical paths in high performance circuits. Thus, it is important to also consider the switching speed within the operation case in order to evaluate the applicability of the new device level approach. Comparing the magenta lines in Figures 4(d) and (h) it is evident, that the CMOS circuit responds much faster in the operation case. This is a result of the relatively high Schottky barrier of 0.64 eV present at the natural NiSi$_2$ to i-Si interface of the MIGFET. Typically, such a near midgap barrier is used to optimize the devices for reconfigurable operation [22]. This means in effect that n-type and p-type program are equally strong as shown by the diamond shaped data points in Fig 6. However, in the present case, where a MIGFETs is used to suppress the charge sharing effect, the feature of reconfigurability is not needed, as the program gate is hardwired to the supply potential. In turn, it is possible to increase the performance of the n-type program at the expense of the p-type performance. The most straightforward way of doing this is by lowering the Schottky barrier height of the source and drain contacts, as already explored in Ref. [11].

Simultaneously, charge sharing is still well suppressed (Fig. 4(g)). Note, that a similar optimization into the opposite direction is possible, i.e. one may increase the on-current of the p-type program of the transistor (circular data points in Fig. 6). Further skewing into one or the other direction can be achieved by using source and drain materials with different workfunctions to each other, in order to obtain a work function offset between source and drain contact, as already explored in 2-D Materials [26], [27].

Beyond this, it has been demonstrated that germanium and silicon-germanium channel materials further reduce $V_{TH}$ and...
increase the on-currents of MIGFETs [28], [29]. Another very straightforward improvement is to apply the clock signal not to a gate aligned on-top of the Schottky barrier, but to one of the channel gates, which perform slightly better even under skewed conditions, as discussed earlier in this section.

B. Topology Analysis

Dynamic gates built from MIGFETs exhibit some notably different topological features than dynamic gates built from classical MOSFETs. In order to demonstrate this the method of logical effort [30] will be applied here. It is a simple and fast circuit design methodology that decouples the intrinsic delay from the delay arising from the topology of a circuit. Albeit very simplistic, it can be used to calculate a good first order approximation of the circuit level effort. The method relies on a simple basic assumption: that the contribution of any logic gate to the propagation delay is split into two fractions: intrinsic inverter delay $\tau$ and normalized circuit delay $d$. While $\tau$ contains all performance measures due to technology scaling, process conditions and applied supply voltage, $d$ yields a normalized value only dependent on the circuit layout. It can be given as:

$$d = gh + p,$$

where $h$ is the fanout and $p$ is a measure for the parasitics. Finally, $g$ is called logical effort, which will be used as a direct measure for the logic gates topological complexity in this analysis. More details about the method itself are described in Ref. [30]. A routine how to calculate logical effort values for logic gates based on RFET and MIGFET technologies can be found in Ref. [16] and Ref. [18].

The calculated logical effort values $g$ for a number of dynamic NAND and NOR logic gates are summarized in Table I. Note that these values are always calculated per input. When looking at CMOS designs first, it is evident that the logical effort of simple dynamic NAND gates increase with $N/3$, where $N$ is the number of inputs. If the gates are footed, meaning there is a clock evaluation transistor in the PDN, the effort increases to $(N + 1)/3$. This increase is reasoned in the increasing topological complexity of long serial paths in classical CMOS technology. For the same reason, NOR gates (as shown in Fig. 7(a,b)) are preferred over NAND gates in dynamic CMOS designs because wide parallel arrangements scale more profitably in terms of performance, which is expressed by the fact that $g$ is independent of the number of inputs. However, footed gates perform much worse than simple non-footed gates.

As opposed to this, MIGFET circuits are especially profitable when long serial paths can be exploited to merge multiple transistors into a single one. As a result, all dynamic NAND gate variants in MIGFET technology show a constant effort of $1/2$ independently of the stack height or the presence of a clock signal, as long as all signals are fed into a single transistor. This is mainly because of the internal resistance of the devices, which also does not scale with the stack height due to being rather limited by the Schottky barrier contacts. On the other hand, the typical NOR arrangements with parallel transistors are detrimental with MIGFETs, albeit showing a constant $g$ per input. Moreover, as each individual input needs an additional program gate, the area will be much larger than in its CMOS counterpart. This is especially problematic for footed NOR gates with internal branching (e.g. the dynamic 2-NOR shown in Figure 7(b)), effectively doubling the

<table>
<thead>
<tr>
<th>GATE</th>
<th>LOGICAL EFFORT $g$ (footed: with clocked evaluation transistor)</th>
<th>MIGFET</th>
<th>CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>INVERTER</td>
<td>$g$ per input</td>
<td>1/2</td>
<td>1/3</td>
</tr>
<tr>
<td>2-NAND</td>
<td>$g$ per input</td>
<td>1/2</td>
<td>2/3</td>
</tr>
<tr>
<td>3-NAND</td>
<td>$g$ per input</td>
<td>1/2</td>
<td>1</td>
</tr>
<tr>
<td>4-NAND</td>
<td>$g$ per input</td>
<td>1/2</td>
<td>4/3</td>
</tr>
<tr>
<td>2-NOR</td>
<td>$g$ per input</td>
<td>1/2</td>
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<td>3-NOR</td>
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<td>4-NOR</td>
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<td>2-NOR</td>
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<td>3-NOR</td>
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<tr>
<td>4-NOR</td>
<td>$g$ per input</td>
<td>1/2</td>
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![Figure 7](image_url)

Figure 7. Dynamic 2-NOR gate variants. (a) Circuit schematic of a simple dynamic 2-NOR gate built from a parallel PUN from classical CMOS and (b) a footed dynamic 2-NOR gate with classical CMOS devices. (c) A dynamic 2-NOR gate in MIGFET technology employing a serial PUN and (d) corresponding circuit layout with a clock signal applied to one of the channel gates.
topological complexity. However, due to the DeMorgan transformation rules, it is also possible to design dynamic logic gate employing a long serial PUN to implement the NOR function (Fig. 7 (c,d)). In classical MOSFET technology, this variant is typically avoided because long serial stacks of p-FET lead to a high topological complexity. With the MIGFET approach proposed here, the device can be individually tuned to a similar performance as the corresponding n-type device (compare also the circular symbols in Fig. 6). As a result, a dynamic NOR gate employing a serial PUN exhibits the same low topological complexity as its NAND gate counterpart employing a serial PDN. The footed NOR designs even show a lower complexity than their CMOS counterparts having a parallel PDN, while the un-footed variants still perform best in classical CMOS designs.

C. Design Example

In the previous section it was demonstrated how the different features of MIGFETs and MOSFETs lead to a different topological complexity at the circuit level. In this section, a simple design example will show how these topology improvements translate into circuit performance. Figure 8 shows the CMOS and MIGFET schematics for a 6-AND domino gate. In both variants two footed dynamic 3-NAND gates are combined with a simple static NOR gate. As all inputs are symmetric, the normalized delay of the critical path \( d_{crit} \) can be calculated by:

\[
d_{crit} = N(h \prod g_i b_i)^{\frac{1}{h}} + \sum p_i \quad (3)
\]

Where \( N \) is the number of stages within the path, \( g_i \) and \( p_i \) are the logical effort and parasitic values of the individual stages, respectively, \( h \) is the fanout of the whole path, and \( b_i \) is the branching effort of every stage. The branching effort thereby is calculated as the on-path capacitances divided by the overall capacitances at each stage. The calculated critical delay results for both circuit variants are shown in Fig. 8(c) as a function of the fanout. It is obvious that the MIGFET variant performs better at the circuit level than the CMOS variant. This benefit originates from the lower logical effort, i.e. the lower complexity of the long serial PDNs, but also from the lower branching effort due to eliminating the need for additional keeper circuits. This benefit scales with large fanouts and yields about 50% reduction in circuit delay at a fanout \( h = 4 \). Slightly reinterpreting this result, one can state that a MIGFET based 6-AND domino gate will perform roughly as well as the CMOS variant, if the underlying device technology reaches 50% of the CMOS device performance.

However, as stated beforehand, this analysis is very simplistic and fails to capture two important effects. The first is velocity saturation, which will lead to a certain overestimation of the resistance of long transistor stacks. The other is the lower switching threshold of dynamic gates as compared to static gates. A dynamic gate will switch as soon as the input rises to \( V_{TH} \), rather than all the way up to \( V_{DD}/2 \), which is assumed as switching point to measure the propagation delay in logical effort theory. As a result both variants will perform slightly different than calculated in this simple design example depending on the actual \( V_{TH} \) and mobility values of the technology. However, the general trend in circuit topology and critical delay reduction at the circuit level will still hold true. This circuit level performance increase comes with the added benefit of being an inherent charge-sharing-free technology, which will lead to more stable circuit operation as well as lower area due to less overhead circuitry.

VI. CONCLUSION

To summarize, it was shown that field effect transistors with multiple independent gates (MIGFETs) provide a simple and CMOS compatible, yet powerful solution to mitigate the charge sharing problem in dynamic logic gates. The unique operation principle of those devices enables the elimination of charge sharing without the need for additional circuity. It allows for larger stacking height of the evaluation network and reduced charge leakage. Examples of circuit layouts of dynamic 2-NAND and 2-NOR gates have been discussed. Suppression of charge sharing, performance and topology have been evaluated based on mixed-mode simulations and logical effort analysis. It has been proposed that dynamic MIGFET gates scale much better with the number of inputs when used to merge long serial networks into a single device. A 6-AND domino circuit has been discussed as one particular design example benefiting from the MIGFET technology. Up to 50% reduction of critical delay has been predicted, all while

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Figure 8. 6-AND domino circuits. Circuit schematics for 6-AND functionality built with (a) classical CMOS and (b) MIGFET. (c) Normalized critical circuit delay comparison of both as resulting from logical effort analysis.
needing less circuitry and avoiding charge sharing. Work function tuning has been proposed among other options to be an efficient method for increasing the on-currents of the individual devices in order to yield competitive overall performance.

REFERENCES


