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Gate-Tunable Negative Differential Resistance in Next-Generation Ge Nanodevices and their Performance Metrics

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In the quest to push the contemporary scientific boundaries in nanoelectronics, Ge is considered a key building block extending device performances, delivering enhanced functionalities. In this work, a quasi-1D monocrystalline and monolithic Al–Ge–Al nanowire heterostructure are embedded into a novel field-effect transistor architecture capable of combining Ge based electronics with an electrostatically tunable negative differential resistance (NDR) distinctly observable at room temperature. In this regard, a detailed study of the key metrics of NDR in Ge is presented. Most notably, a highly efficient and low-footprint platform is demonstrated, paving the way for potential applications such as fast switching multi-valued logic devices, static memory cells, or high-frequency oscillators, all implemented in one fully complementary metal–oxide–semiconductor compatible Al-Ge based device platform.

1. Introduction

The continuous downscaling of the Si-based planar metal oxide field-effect transistor (MOSFET) integrated circuit technology has been the main driving force to reduce the size, power consumption, and cost of modern microelectronic devices.[1] However, despite the continuous advancement in nanofabrication and electronic device geometries, fundamental scaling limits will restrict further performance enhancement.[2] At the same time, emerging distributed computing paradigms such as the Internet of Things[3] are placing extraordinarily stringent constraints on hardware performance, forcing a shift of research efforts towards the integration of new materials, processes, and device architectures.[4–6] In this context, low-dimensional Ge structures such as nanomembranes[7,8] and vapor-liquid-solid[9] (VLS) grown nanowires[10,11] (NWs), exhibiting unique electrical[4,10,12] and optical[13–15] properties departing from their bulk counterparts, are considered key building blocks in a "More than Moore" approach extending device performances beyond the limits imposed by miniaturization.[16,17] In this respect, a highly interesting transport mechanism is the transferred electron effect, enabling negative differential resistance (NDR) following the Ridley–Watkins–Hilsum theory.[18] Also known as the Gunn-effect in GaAs[19] and GaN nanocrystals,[20] this effect is based on applying sufficiently high electric fields, resulting in electrons from the energetically favorable conduction band valley, characterized by a low effective mass, being transferred to a heavy mass valley nearby.[19] The unique NDR characteristic can be exploited for novel logic gates providing a significant advantage over conventional logic devices in one or more performance metrics such as area, speed, or power.[21] In this respect, the monostable-bistable transition logic element (MOBILE) is a functional logic gate employing two NDR devices connected in series and was shown to perform both NAND and NOR operations.[21,22] However, the monolithic integration of large foot-print group III-V based NDR devices on a Si platform is challenging.[22] Despite pioneering work demonstrating NDR in Ge, until now, the observation was either limited to low temperatures,[23,24] impracticable for typical applications, the exploitation of the transient behavior of surface traps,[25] plasmon-induced hot electron injection[26] or required careful preconditioning of the Ge surface.[27]

In this work, we systematically analyze NDR at room temperature based on the transferred electron effect in Al-Ge-Al NW heterostructures. The reproducible and reliable device fabrication combined with a low foot-print and stable device operation enabled the extraction of the key parameters of NDR in Ge providing a significant step towards potential applications such as fast switching logic circuits, static memory cells, or high-frequency oscillators.[21]

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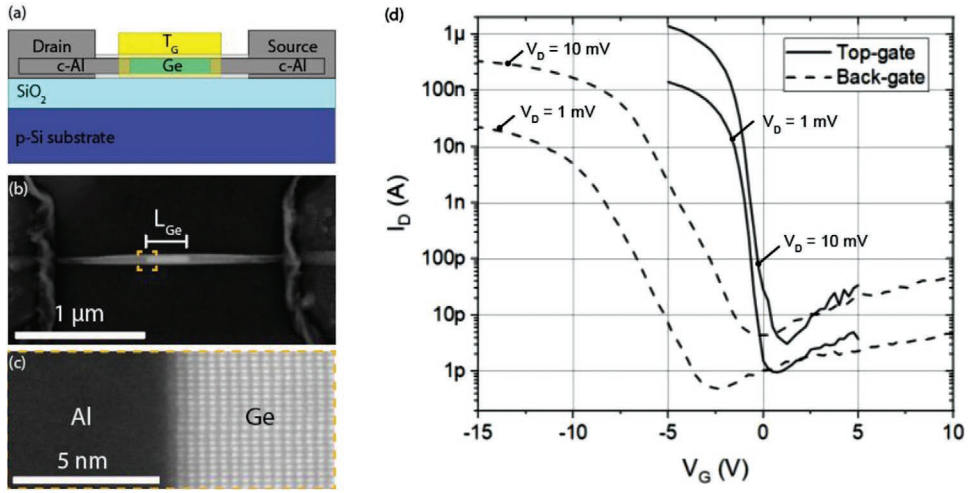

Figure 1. a) Schematic of a top-gated Al-Ge-Al NW heterostructure device. b) SEM image before top-gate fabrication. The length and diameter of the actual Ge channel is L_{Ge} = 256 nm and d_{NW} = 30 nm, respectively. c) HAADFSTEM image showing a zoom-in at the Al-Ge interface region. d) Transfer characteristic of a back-gated (dashed lines) and top-gated (solid lines) Ge NW FET device for a bias of V_D = 1 and 10 mV.

2. Results and Discussion

To investigate the electrical properties, nominally intrinsic VLS-grown Ge NWs with diameters between 25 and 50 nm were integrated into field-effect transistors (FETs) (see **Figure 1**a). For device fabrication, a thermally induced exchange reaction between the NWs and Al contact pads was used to achieve Ge segments contacted by self-aligned, single crystalline Al NW leads[28] with atomically sharp and flat heterojunctions (see Figure 1b).[29] Due to the large surface to volume ratio, adsorbates and surface states have a significant impact on the electrical characteristics of NW-based devices.[30,31] Consequently, to ensure reliable and reproducible electrical measurements, the NWs were enwrapped in a protective 20 nm thick atomic layer deposition (ALD) grown Al_2O_3-insulator shell.[25] Without contact annealing, the device characteristic appeared to be a statistic process resulting in either p-type, n-type, or ambipolar operation (see Figure S1, Supporting Information). This variability can be attributed to a residual (and patchy) parasitic oxide-layer on the contact area between the Ge NW and the Al pads that is indeed known to have a significant influence on the transport properties of nanoscale devices.[32] Figure 1c shows the unique atomically sharp interface of the fabricated Al-Ge-Al longitudinal NW heterostructure based on high angle annular dark-field (HAADF) scanning transmission electron microscopy (STEM). The image confirms that our NW axis is oriented along the ⟨111⟩ crystallographic direction. Further, details regarding the fabrication process of our Al-Ge-Al NW heterostructures used for other electronic applications, as well as physical analysis, that is, high-resolution transmission electron microscopy (HR-TEM) and energy dispersive X-ray spectroscopy investigations can be found in the work of Kral et al.[29] and El Hajraoui et al.[33]

Using the Si substrate as global back-gate, nominally intrinsic Ge NWs enwrapped in a protective Al_2O_3-shell exhibit a slight ambipolar behavior, with predominant hole transport for negative gate voltages (see dashed curves in Figure 1d).[11] It has been noted that surface doping,[34] due to acceptor-like traps, results in a shift of the energy band structure throughout the entire NW cross-section, causing predominant p-type behavior in nominally intrinsic Ge NWs.[35,30] Exemplary for the evaluation of more than 25 similar heterostructure devices (see Figure S2, Supporting Information), the transfer characteristic shown in Figure 1a reveals that even applying ultra-low drain voltages down to V_D = 1 mV, an I_{ON}/I_{OFF} ratio increasing from 10^4 to 10^5 can be achieved with our devices while only showing a slight ambipolar behavior. Next, the effective Schottky barrier height for electrons for the injecting Al-Ge junction was estimated. Assuming thermionic emission, the total activation energy of the system at small biases was determined. Different to Schottky diodes in Schottky FETs, the actual potential drop across the junction is unknown from IV measurements. Thereto the slope of the activation energy plot of $\ln(J\,T^{-2})$ versus $1000/T$ at various bias voltages (see Supporting Information) was employed. The thereof estimated barrier height in the sub-threshold region of the electron-dominated transport was estimated to be 196 ±25 meV, which is in perfect agreement with the theoretical value of the Schottky barrier height of 200 meV for bulk Al-Ge Schottky junctions.[36] To improve the electrostatic control of the Ge channel and to decrease the absolute value of the applied gate voltage, an omega-shaped top-gate was fabricated atop the Al_2O_3 coated Ge channel. In this configuration, the I_{ON}/I_{OFF} ratio could be improved by one order of magnitude to 10^5–10^6 (solid lines shown in Figure 1d). Additional transfer curves of heterostructure devices with channel lengths of L_{Ge} = 150 to 759 nm are shown in Figure S6, Supporting Information. For our top-gated devices an enhanced sub-threshold swing of $SS = \mathrm{d}[\log(I_D)] / \mathrm{d}V_{TG}$ = 300 ±50 mV/decade was extracted.

To gain access to the electron-dominated transport regime positive back-gate voltages of V_{BG} = 5, 15, and 30 V were applied. The corresponding I/V measurements were recorded by linearly increasing V_D while monitoring I_D (**Figure 2**a). For a positive V_{BG} an unambiguous observation NDR is given with progressive enhancement for higher V_{BG}. The respective band diagram is shown in the left inset of Figure 2a. For V_{BG} ranging

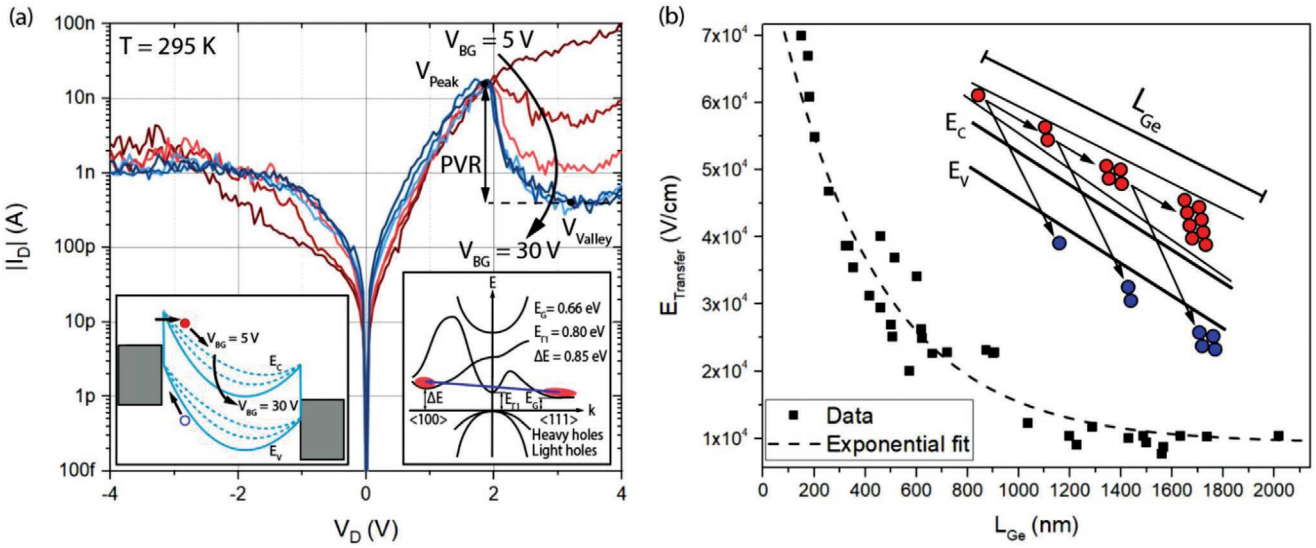

Figure 2. a) Semi-logarithmic I/V characteristic recorded for different back-gate voltages between V_{BG} = 5 and 30 V of an Al-Ge-Al NW heterostructure device with L_{Ge} = 450 nm. Shifting the device characteristic to n-type operation, clear signatures of NDR are visible. The left inset shows the respective schematic band diagram for applying a positive V_D to the heterostructure device, resulting in electrons being injected by a combination of Fowler–Nordheim tunneling and thermionic emission. The large bias voltage across the semiconductor and the downward bent bands enable the electron transfer from the L- to the Δ-valley. The right inset shows the band diagram of Ge with the electric field induced electron transfer from the ⟨111⟩ valley into the ⟨100⟩ valley enabling NDR, diagram adapted from ref. [46]. b) $E_{Transfer}$ as a function of the Ge channel length L_{Ge}. The inset is showing a schematic illustration of charge carrier scattering in the Ge channel.

between 5 and 30 V, the increasing downward band bending results in a thinning of the barrier width for electron injection at the source electrode. As a consequence electron injection through Fowler–Nordheim tunneling is expected to occur in addition to thermionic emission, delivering an enhancement of electron injection into the channel. This band-tuning effect is stronger for thinner NW diameters and higher gate capacitances. In this configuration, we interpret the observations as follows. Hot electrons are scattered from the energetically favorable conduction band valley, characterized by a low effective mass to a heavy mass valley nearby.[19] Although the Γ-point minimum in Ge is energetically closer to the L-point minimum, the coupling constant between ⟨111⟩ and ⟨000⟩ minima is significantly lower than between ⟨111⟩ and ⟨100⟩ minima.[37] Consequently, as schematically illustrated in the right inset of Figure 2a, the transferred electron effect in Ge is most likely to apply for the L-point and Δ-point minima of the ⟨111⟩ and ⟨100⟩ sub-bands of the conduction band with the respective effective masses of $m^*_{L,t}$ = 0.082 m_0 and $m^*_{\Delta,t}$ = 0.288 m_0.[37] Figure S7, Supporting Information, shows a series of consecutive I/V measurements to demonstrate the stability of the NDR operation of our devices. Figure S8, Supporting Information, shows the current density at V_{Peak} (J_{Peak}) of 24 similar Al-Ge-Al heterostructures in dependence of the Ge channel length and the NW diameter. With an average J_{Peak} of 2 kA cm^{-2} at room-temperature, our devices reveal three orders of magnitude higher value compared to larger footprint Ni/n+ Ge diodes[23] even when operating at T = 230 K. According to the nature of the transferred electron effect, measuring the I/V characteristic for V_{BG} = 30 V, sweeping V_D first from –4 to 4 V and back from 4 to –4 V, results in the NDR being observed in the negative branch of the I/V characteristic (see Figure S9, Supporting Information).[38]

Further, Figure 2b shows the dependence of the electric field ($E_{Transfer}$) required to carry out the proposed electron transfer from the ⟨111⟩ to the ⟨100⟩ minima. The evaluation of Al-Ge-Al devices with L_{Ge} between 150 nm and 2 µm revealed that a relatively constant electric field of $E_{Tansfer}$ = 1 × 10^4 V cm^{-1} appeared to be sufficient for devices with L_{Ge} > 1 µm to initiate the electron transfer. However, with ever shorter Ge channel lengths, an exponential increase of the electric field close to the breakdown field for bulk Ge with E_C = 100 kV cm^{-1}[39] was found. As schematically illustrated in the inset of Figure 2b, this finding is consistent with hot electrons releasing their energy gained from the electric field by creating electron-hole pairs, which are subsequently split by the increasing electric field. The continuation of this process results in highly energetic electrons and thus an increased rate of electrons being transferred to the ⟨100⟩ valley. However, with ever-decreasing channel lengths, the acceleration path is decreasing, resulting in less energetic electrons. Thus, a significantly higher $E_{Transfer}$ is required to initiate NDR in short channel devices.

Next, we focus on the NDR figure-of-merit (FOM) parameters of our Al-Ge-Al NW heterostructures. **Figure 3** shows a semi-logarithmic I/V characteristic showing the NDR recorded for a fixed back-gate voltage of V_{BG} = 30 V. The most important parameter of NDR devices is their peak-to-valley ratio (PVR), which is defined by PVR = $I(V_{Peak})$ / $I(V_{Valley})$. We found that with respect to the back-gate voltage, the PVR in our devices can be tuned. In conjunction with an increased accumulation of electrons, tuning the back-gate voltage from V_{BG} = 10 to 30 V dramatically increases the PVR from 2.5 to 27.5. Figure 3a shows the temperature dependence of the NDR of a heterostructure device with L_{Ge} = 450 nm, recorded at a constant back-gate voltage of V_{BG} = 30 V for T = 200, 295, and 350 K.

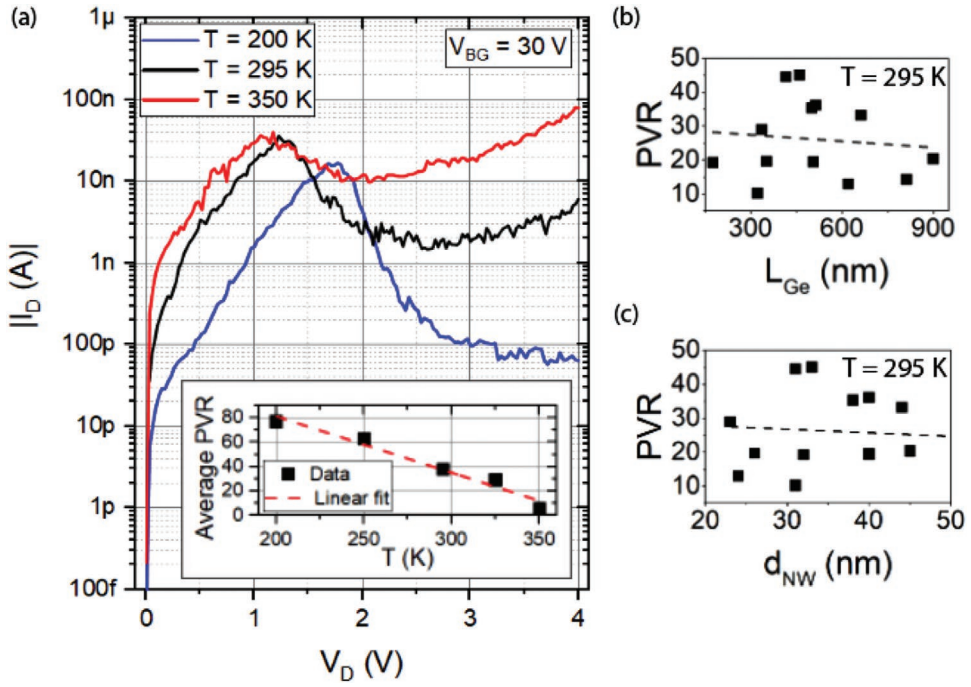

Figure 3. a) Semi-logarithmic I/V characteristic recorded for V_{BG} = 30 V an Al-Ge-Al NW heterostructure device with L_{Ge} = 450 nm, recorded at T = 200, 295, and 350 K. The respective PVR values are 220, 25, and 5. The inset shows the average PVR based on the measurement of 10 devices measured at temperatures between T = 200 and 350 K. Dependence of the PVR on b) the Ge channel length NW and c) the NW diameter.

Associated with an increase of the scattering mean free path at low temperatures, the respective PVR values are 220, 25, and 5, accordingly. An evaluation of the average PVR of 10 heterostructure devices for temperatures between T = 200 K and 350 K is supplied in the inset. Linearly fitting the data, the PVR decreases with a rate of 0.46 K^{-1} within the given temperature range. We want to note that the relatively high back-gate voltage of V_{BG} = 30 V can be reduced to 5 V if a top-gate architecture is used (see Figure S10, Supporting Information). As a substantially larger PVR is desirable for oscillators and diverse digital applications,[21,22] we have systematically evaluated the PVR as a function of the Ge channel length (Figure 3b) and the NW diameter (Figure 3c) of 21 heterostructure devices. In comparison with Ge quantum dot tunneling diodes[40], Si and Si/SiGe resonant interband tunneling diodes,[41,42] the room-temperature PVR of our best performing devices is approximately a factor 20 larger.

With respect to the scalability of the NDR in Ge, we found that heterostructure devices with Ge channel lengths L_{Ge} < 100 nm showed no signs of NDR, which we attribute to the quasi-ballistic[43] nature of such short channel Ge heterostructure devices. Consequently, the best performing devices were found to have d_{NW} = 20 nm and L_{Ge} = 150 nm just over three times longer than the scattering mean free path in our Ge NWs.[43] Compared to state of the art NDR devices, our architecture exhibits an ultra-short footprint. As shown in **Figure 4**a, embedded in the proposed top-gate architecture, these devices can be operated with V_{Peak} = 0.9 V and V_{Valley} = 1.2 V, still providing a PVR of 4.5 at T = 295 K. As shown in Figure 4b,c respectively, a longer Ge channel increases the device resistance, shifting V_{Peak} and V_{Valley} to higher voltages. With respect to oscillator devices, NDR metrics such as V_{Span} = (V_{Peak} − V_{Valley}), the conductance slope ($|G_{Slope}|$), characterizing the abruptness of the NDR region and the extent of the voltage plateau ($V_{Plateau}$), defined as the width of the valley, are of utmost importance.[21] V_{Span} is used to characterize the voltage window of the NDR region, with a larger voltage being preferred for oscillator applications, as the maximum oscillation power is proportional to V_{Span}.[22] We found a maximum of V_{Span} = 2.2 V for devices with L_{Ge} = 900 nm. In conjunction with both, $|G_{Slope}|$ and $V_{Plateau}$ being significantly larger for long Ge channels, heterostructure devices with L_{Ge} > 700 nm, seem to be better suited for oscillator applications.

The performed systematic benchmark of the NDR metrics in Al-Ge-Al NW heterostructures embedded in FET architectures revealed their high potential as a low-footprint platform enabling both, logic and oscillator applications. Highly relevant for a cost-efficient practical implementation, our approach presented here can be transferred into a fully complementary metal–oxide–semiconductor (CMOS) compatible Al-Ge based device platform paving the way for an unprecedented realization of circuits based on monolithically integrated gate-controlled NDR transistors with conventional MOSFETs.

3. Conclusion

In conclusion, we have thoroughly analyzed the NDR effect in Al-Ge-Al NW heterostructures embedded in the back- and top-gated FET architectures. Based on the evaluation, the NDR FOM metrics could be extracted. Most notably, the versatility of our Al-Ge-Al NW heterostructures provides a platform

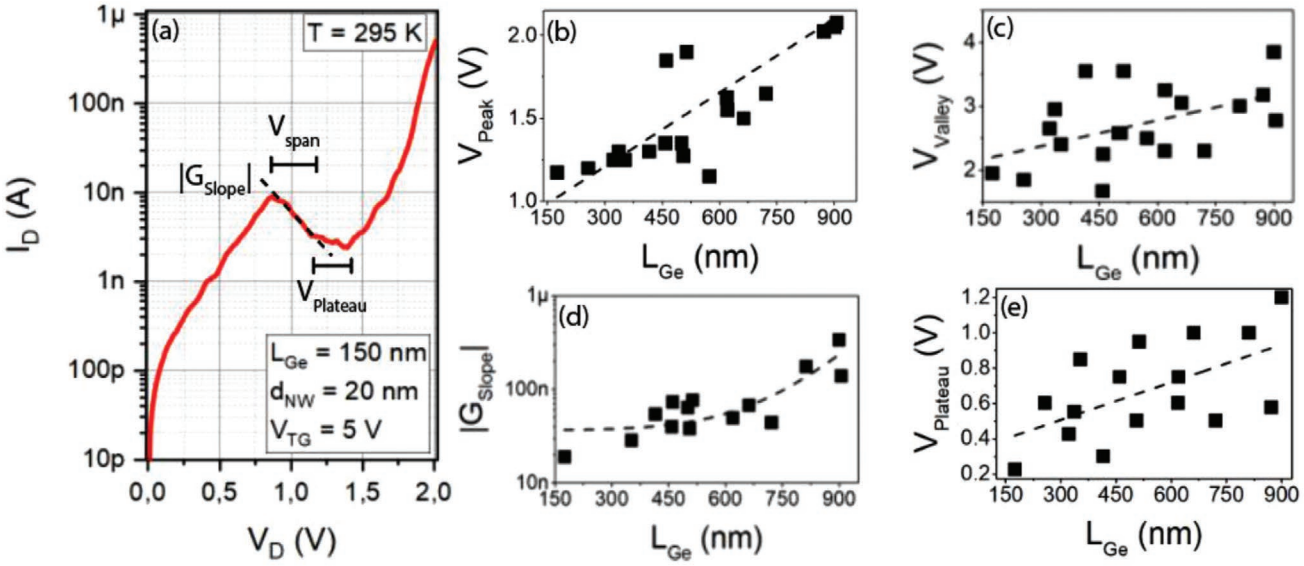

Figure 4. a) Semi-logarithmic I/V characteristic of an ultra-scaled top-gated Al-Ge-Al heterostructure NDR device with $L_{Ge} = 150$ nm and $d_{NW} = 20$ nm recorded for a top-gate voltage of $V_{TG} = 5$ V. The important NDR FOM metrics $|G_{Slope}|$, V_{Span}, and $V_{Plateau}$ are indicated. b–e) Dependence of V_{Peak}, V_{Valley}, $|G_{Slope}|$, and V_{Span} on L_{Ge}. The data were measured at ambient conditions at a temperature of $T = 295$ K.

extending Ge based electronics with NDR applications such as fast switching logic circuits, static memory cells, or high-frequency oscillators. In this respect, we believe that our investigations provide a significant step towards a beyond CMOS approach enabling functional diversification and alternative computing for the post-Si era.

4. Experimental Section

Synthesis of Ge NWs: The used Ge NWs were grown on Si (111) substrates using the VLS growth mechanism with mono-germane (GeH_4, 2% diluted in He) as precursor and a 2 nm thick sputtered Au layer as the 1D growth-promoting catalyst and seed. The actual growth was performed using a low-pressure hot-wall CVD chamber at a total pressure of 50 mbar and a gas flow of 100 sccm for both the precursor gas and H_2 as the carrier gas. After stabilizing the pressure and precursor gas flow, the temperature was ramped up at a rate of 110 K min^{-1} to the target temperature of 614 K. The rather high growth temperature ensures uniform catalyst diameter and good NW epitaxy. After a 10 min nucleation phase, the temperature was lowered to 573 K. Typical growth duration of 60 min resulted in 8 µm long NWs and uniform diameters of about 30 nm. Subsequently to the growth, the NWs were uniformly coated with a 20 nm thick Al_2O_3-shell[26] by ALD at a temperature of 473 K.

Device Fabrication: The starting materials were VLS grown Ge NWs with diameters of approximately 30 nm coated with 20 nm high-k Al_2O_3 using ALD. The passivated Ge NWs were drop-casted onto a 100 nm thick thermally grown SiO_2 layer atop of a 500 µm thick highly p-doped Si substrate acting as a common back-gate. The Ge NWs were contacted via Al pads fabricated by electron beam lithography, 100 nm Al sputter deposition, and lift-off techniques. A successive thermally induced exchange reaction by rapid thermal annealing at a temperature of $T = 624$ K in forming-gas atmosphere initiated the substitution of Ge by Al.[29,33,43] Facilitating this heterostructure formation scheme allowed the integration of single-crystalline monolithic Al-Ge-Al NW heterostructures with tunable channel lengths in a back-gated FET architecture. Further, omega-shaped Ti/Au top-gates were fabricated using a combination of electron beam lithography, Ti/Au electron beam evaporation (8 nm Ti, 125 nm Au, deposition rate 0.05 nm s^{-1}, and base pressure 2×10^{-7} mbar), and lift-off techniques.

High-Resolution HAADF STEM: HAADF STEM was performed on Al-Ge-Al NW heterostructures fabricated on 40 nm thick Si_3N_4 membranes[44,45] using a probe-corrected FEI Titan Themis, working at 200 kV. The Al-Ge interface in the shown images lies along the [112] direction of observation of the Ge crystal.

Electrical Characterization: The electrical measurements were carried out at room temperature and ambient conditions using a combination of a semiconductor analyzer (HP 4156B) and a probe station. To minimize the influence of ambient light as well as electromagnetic fields, the probe station was placed in a dark box. Temperature-dependent measurements (200–350 K) were performed in vacuum at a background pressure of approximately 5×10^{-6} mbar using a cryogenic probe station (LakeShore PS-100) and a semiconductor analyzer (Keysight B1500A).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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R.B. and M.S. contributed equally to this work. M.S. and M.G.B. performed the device fabrication. R.B., M.S., and K.E. conducted the measurements. M.S. wrote the manuscript. M.A.L. and M.I.H. carried out the TEM characterization and analysis. A.L. provided helpful feedback and commented on the manuscript. W.M.W conceived the project and contributed essentially to the experimental design. All authors analyzed the results and helped shape the research and manuscript. The authors gratefully acknowledge financial support by the Austrian Science Fund (FWF): project No.: P29729-N27. The authors further thank the Center for Micro- and Nanostructures for providing the cleanroom facilities.

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

Research data are not shared.

Keywords

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