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## ABSTRACT

The implementation of advanced electronic devices in the fourth industrial revolution era can be achieved with bottom-up grown silicon nanowire (Si-NW) based transistors. Here, we have fabricated reconfigurable Schottky-barrier (SB) thin-film transistors (TFTs) consisting of a parallel array of bottom-up grown single-crystalline Si-NWs and investigated in detail their device length dependent electrical performance and transport mechanism with current–voltage transport-map, key electrical parameters, and numerical simulation. In particular, the effective extension length ($L_{ext\_eff}$) limited significantly the overall conduction behavior of reconfigurable Si-NW SB-TFTs, such as ambipolarity, mobility, threshold voltage, and series resistance. This work provides important information for a better understanding of the physical operation of reconfigurable transistors with SB contacts and further optimization of their performance for implementing practical applications.



## INTRODUCTION

Tunnel field-effect transistor (FET), Fin-FET, gate-all-around (GAA) nanowire FET, and ultrathin body (UTB) transistor have received considerable attention for improvement of device power, performance, area, and cost (PPAC), while minimizing short-channel effects (SCEs).[1–4] Bottom-up grown single-crystalline silicon nanowire (Si-NW) based FETs are also attractive candidates for the realization of next generation display, sensor devices, and wearable electronics in the fourth industrial revolution era, described as the Internet of things (IoT), advanced mobile devices, artificial intelligence (AI), and cloud computing.[5–10] Si-NW can be easily transferred from a growth substrate to diverse substrates including flexible/transparent plastic substrates, and device fabrication is possible under low temperature since dopant activation is not required in the Si-NW based devices. In particular, thin-film transistors (TFT) with Si-NW array have several promising advantages such as high mobility, less material degradation issues, and improved stability due to good interface between channel and insulator, as compared to amorphous-Si, polycrystalline-Si, oxide semiconductor, and organic semiconductor based TFTs.[7,8] In addition, Si-NW based Schottky-barrier (SB) transistors have a steep junction at interfaces between Si-NW and metallic silicides, which allow a typical switching operation without a heavy doping process at source/drain (S/D) contacts in conventional transistors.[11–13] High performance pH-, bio-sensors, and steep-slope transistors for energy efficient system have been successfully demonstrated with the Si-NW SB transistors so far.[14–18] Ambipolar conduction behavior is typically observed in SB transistors since both electron and hole carriers are injected into the Si-NW channel through the silicide junctions. This can lead to a novel multi-functional device, the so-called reconfigurable field-effect transistors (RFETs) with an additional polarity gate[19–23] that allows us to select one of the carrier types only. New complimentary logic circuits with a smaller number of devices, reduced chip area, and low thermal budget can be implemented using the RFETs.[24]

In this paper, reconfigurable SB-TFTs constructed from a parallel array of bottom-up grown Si-NWs with double gate structures

have been fabricated with different channel lengths. Then, their electrical properties and operation mechanism were investigated as a function of the device geometry and various bias conditions. From current–voltage ($I$–$V$) transport-maps, transconductance behavior, and numerical simulations, we showed that the ambipolar behavior and the reconfigurable operation are significantly affected by the extension length of the Si-NW SB-TFTs. Furthermore, polarity gate-bias affected electrical parameters, such as mobility, series resistance, and threshold voltage, were discussed.

## RESULTS AND DISCUSSION

Figure 1 exhibits scanning electron microscopy (SEM) images and a schematic view of the completed devices. The device length (L) between source and drain electrodes [see Fig. 1(d)] ranged from 3 to 16 $\mu$m, and the channel length ($L_{ch}$) was fixed at 2 $\mu$m. An abrupt $NiSi_2$/Si Schottky-junction is clearly observed in the SEM image at the bottom of Fig. 1.

Transfer curves (drain current $I_d$ vs front-gate voltage $V_{gf}$) of the Si-NW SB-TFTs with different device lengths (L) were measured

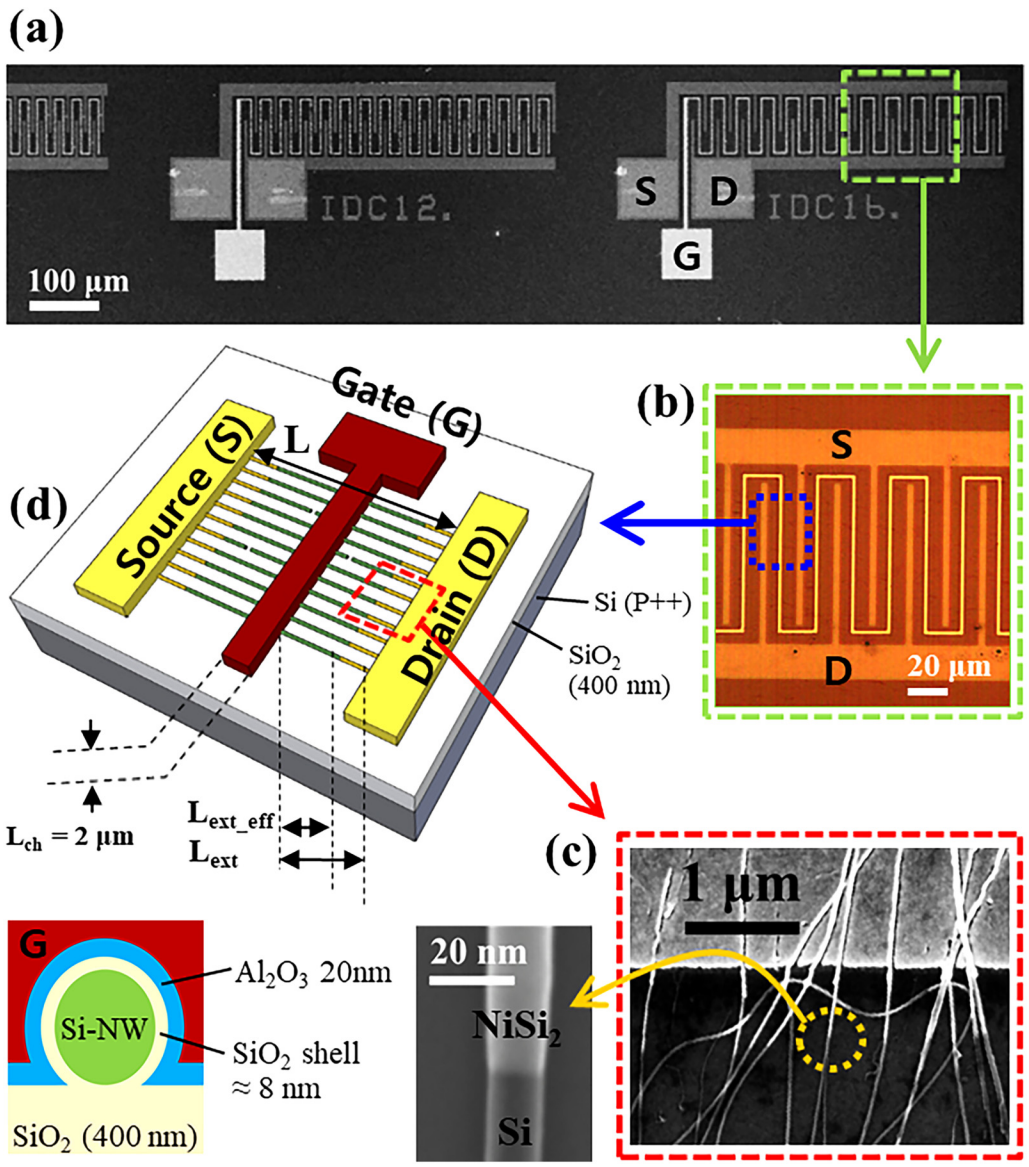


**FIG. 1.** (a) and (c) Scanning electron microscopy (SEM) images, (b) optical microscopy (OM) image, and (d) schematic view of the fabricated Si-NW SB-TFTs. An abrupt $NiSi_2$/Si Schottky-junction was clearly observed in the SEM image at the bottom.

with a small drain bias ($V_d = 50$ mV), as shown in Fig. 2(a). The device with $L = 3\,\mu$m was electrically shorted since whole Si-NWs were fully silicided into $NiSi_2$ (Fig. S1 in the supplementary material). The length of the $NiSi_2$ silicide was also estimated to be close to $3\,\mu$m from the linear relationship between gate-to-channel capacitance ($C_{gc}$) and L in a previous work.[25] Very long channel device ($L = 16\,\mu$m) showed a p-type unipolar transistor characteristic. Although the Si-NW is not intentionally doped during the CVD growth process, the Si-NW channel could still be electrostatically turned into p-type due to the electrostatic force from interface charges and the work function difference between the gate metal and the Si-NW. A Schottky-barrier (SB) is created from the $NiSi_2$/Si-NW hetero-junctions, and the SB height for electrons ($q\Phi_{Be} \approx 0.66$ eV) is greater than that for holes ($q\Phi_{Bh} \approx 0.46$ eV) since the Fermi level of $NiSi_2$ is closer to the valence band of the Si-NW.[21] The surface potential of the silicon is pinned leading to fixed SB at the S/D sides in the long channel device that favors the injection of holes. The hole concentration within the channel is controlled by the control gate voltage $V_{gf}$. Interestingly, the n-branch due to electron conduction appears and increases as the channel length L is reduced. Finally, a typical ambipolar behavior was observed in the device having a device length of $L = 4\,\mu$m, where the $NiSi_2$/Si-NW junctions are fully covered by the front-gate electrode (Fig. S1 in the supplementary material). The surface potential of the silicon nanowire is no longer fixed in the device with $L = 4\,\mu$m, where there is no ungated extension region. The injection probability of holes through SB is raised for $V_{gf} < 0$. The injection of electrons is also enhanced due to the thinned SB width for electrons in the case of $V_{gf} > 0$. The SB junction is not governed by $V_{gf}$, when the effective extension length ($L_{ext\_eff}$) between $NiSi_2$/Si-NW interface and the edge of front-gate electrode is sufficiently long. However, the electric-field (E-field) from the gate can influence the $NiS_2$/Si-NW interface in the device with a short $L_{ext\_eff}$, and the SB junction is modulated by the gate voltage $V_{gf}$.

In addition, the L dependent transconductance ($g_m$) of Si-NW SB-TFTs was investigated. Figure 2(b) shows $g_m$ normalized to its maximum value for different L values. The $g_m$ of a typical SB transistors without the extension part continually increased as increasing $|V_{gf}|$ due to the enhanced hole injection through the reduced

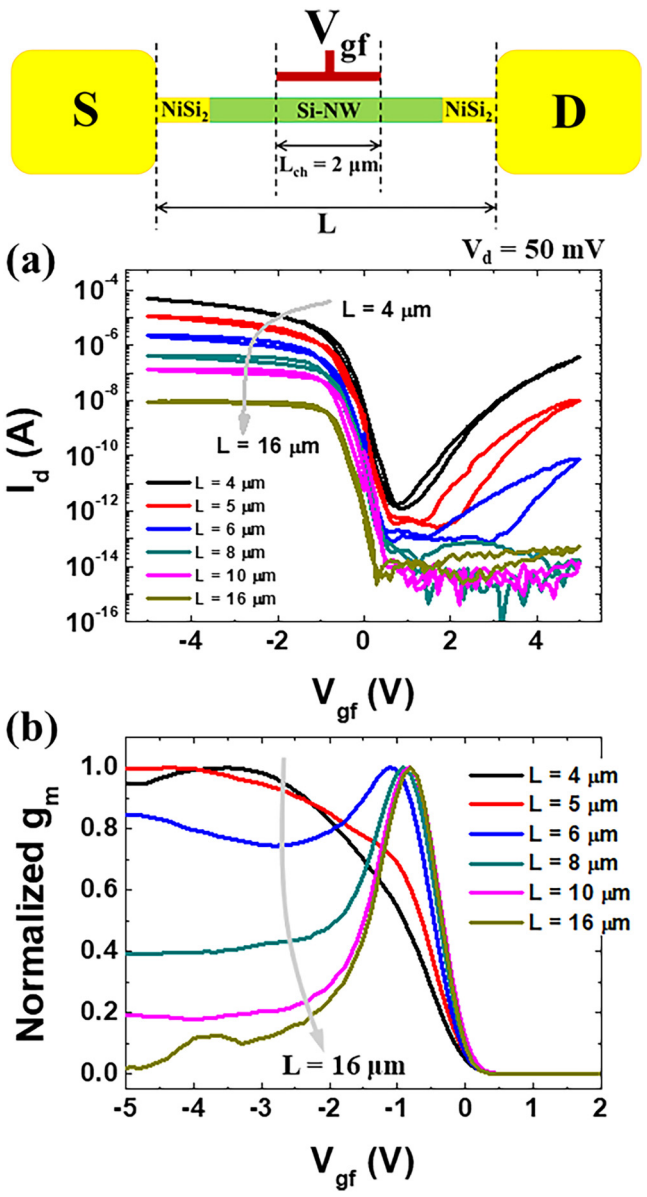


**FIG. 2.** (a) Transfer curves of Si-NW SB-TFTs with varying L and a small $V_d = 50$ mV. A long L device showed a p-type unipolar switching characteristic, while an ambipolar behavior was observed in a short length device. (b) Normalized $g_m$ for different nanowire lengths L. A long L device showed a peak and degradation behavior as increasing $V_{gf}$, while a continuously increased trend was observed in a short length device.

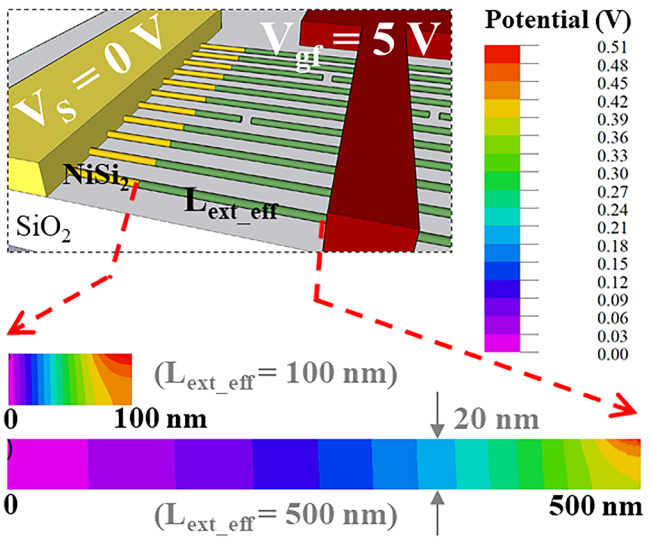


**FIG. 3.** Numerically simulated potential distribution along the Si-NW extension with an extension length of 100 and 500 nm lengths.

width of the SB (see the black and red curves of the device with L = 4 and 5 $\mu$m). The $g_m$ of a long L device with considerable extension and fixed SB in the not gated area shows a peak and degradation behavior for further increasing $|V_{gf}|$ due to an invariant injection of holes, surface roughness scattering, and the extension resistance.[25–27]

Figure 3 shows the simulated potential distribution along the Si-NW extension for different device lengths. FlexPDE software (PDE solutions, Inc.) based on the finite element method was used for the numerical simulations. The potential distribution according to bias conditions was simulated with solving the Poisson equations, and FlexPDE scripts were used for the calculation. The detailed structure and boundary condition for the simulation were described Fig. S2 in the supplementary material. In the case of

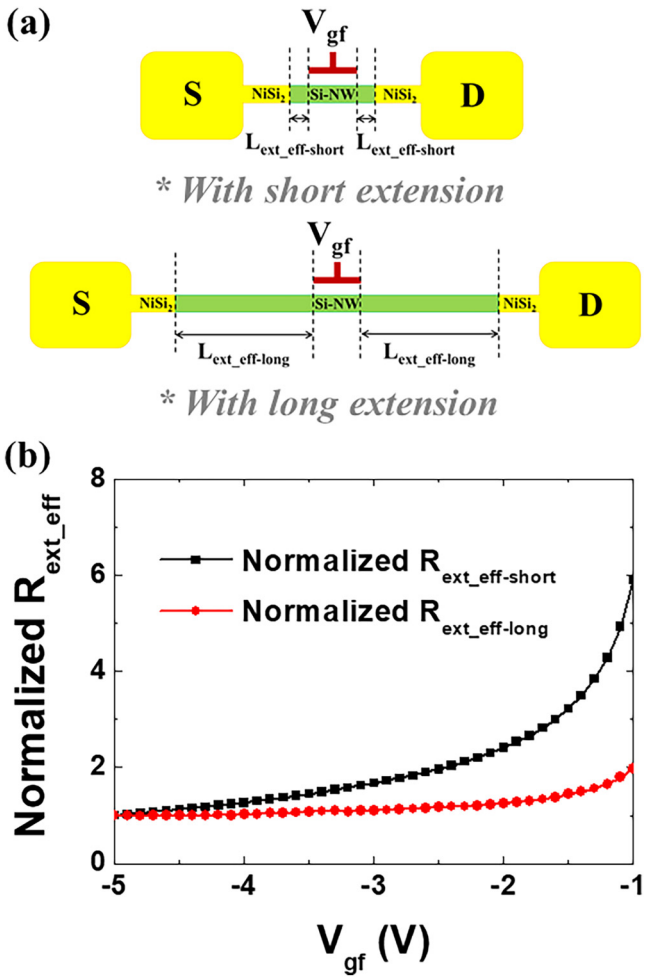


**FIG. 4.** (a) Schematic of a device with short and long extension length. (b) Normalized $R_{ext\_eff}$ vs $V_{gf}$ with the short and the long extension lengths extracted by using the simple subtraction method described Fig. S3 in the supplementary material.

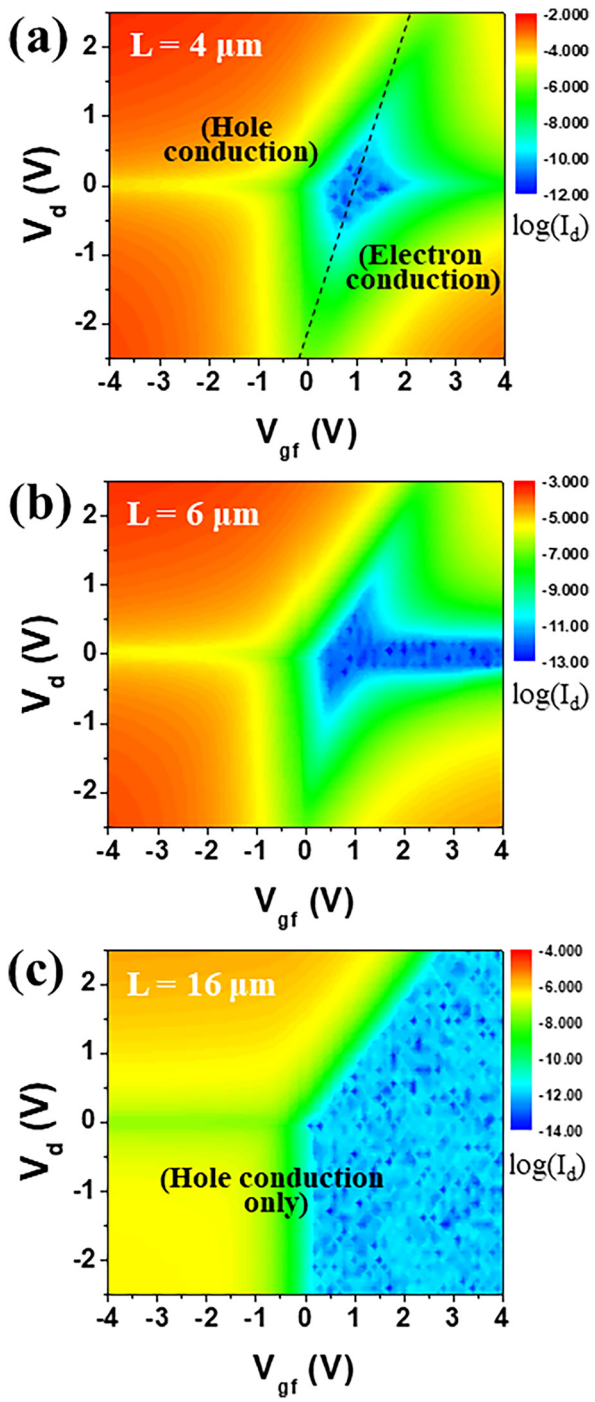


**FIG. 5.** Current–voltage (*I–V*) contour transport-maps of Si-NW SB-TFTs with different device lengths (L). (a) L = 4 $\mu$m, (b) L = 6 $\mu$m, and (c) L = 16 $\mu$m. A typical behavior of an ambipolar SB transistor is observed for L = 4 $\mu$m (a). A pronounced drain-bias dependence of the electron dominant conduction is observed in the device with intermediate L = 6 $\mu$m (b). Only hole carrier dominant conduction is shown for the device with the long length L = 16 $\mu$m (c).

relatively long extension ($L_{ext\_eff}$ = 500 nm), the potential distribution changes smoothly along the extension region. On the other hand, for a short extension ($L_{ext\_eff}$ = 100 nm), the E-field from the $V_{gf}$ resulted in a faster changing potential-gradient between the $NiSi_2$/Si-NW hetero-junction and the edge of the front-gate. Therefore, the potential is also affected even near the hetero-junction in the case of the short extension, and that results in the most pronounced ambipolar characteristics of the device with L = 4 $\mu$m in Fig. 2(a).

$V_{gf}$ effect on the resistance value of the Si-NW extension ($R_{ext\_eff}$) was discussed in Fig. 4. The total resistance ($R_{tot} = V_d/I_d$) of the Si-NW SB-TFTs can be determined by $R_{ch} + 2 \times (R_{ext\_eff} + R_{NiSi})$,

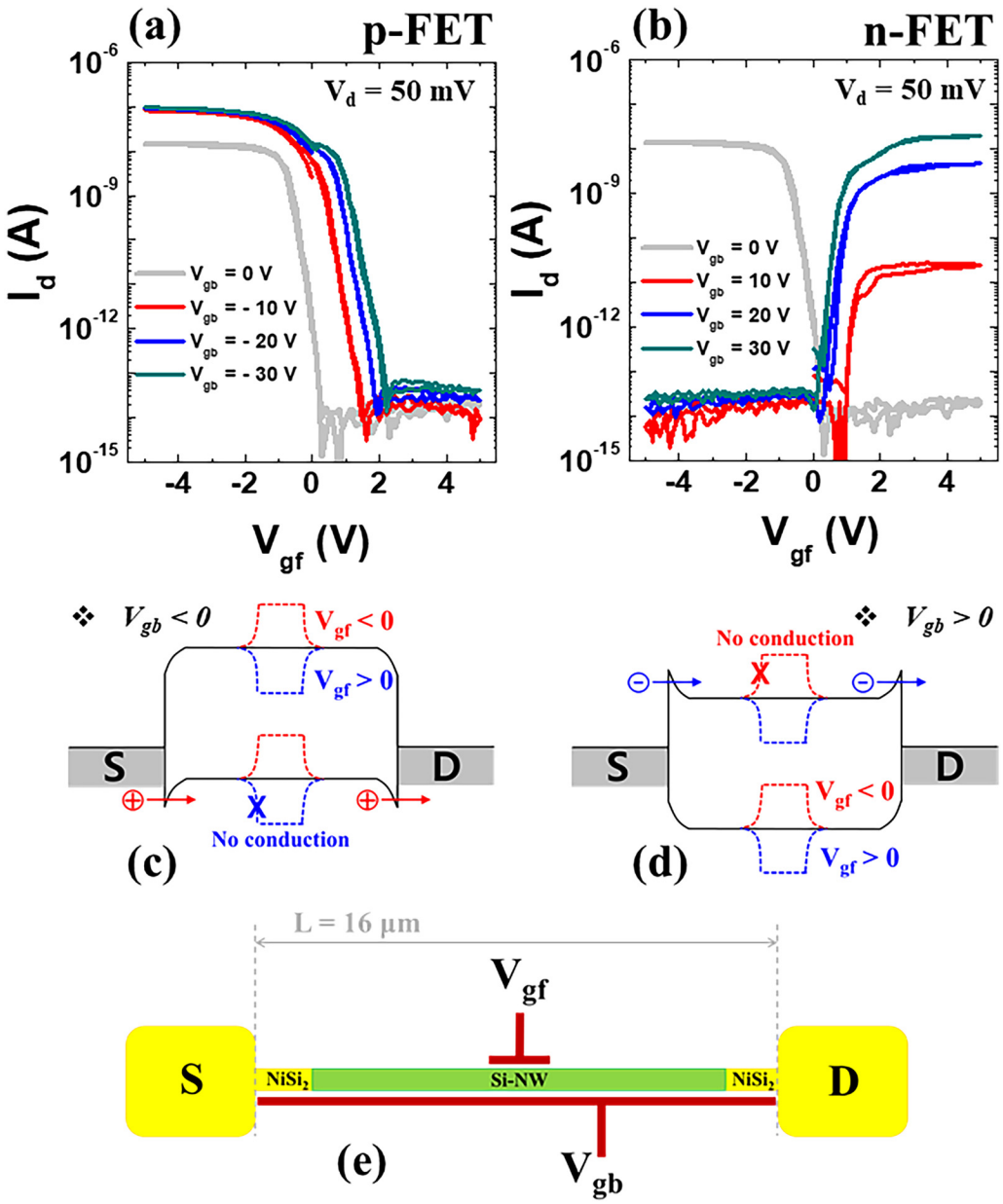


**FIG. 6.** Reconfigurable transfer curves for (a) p-type and (b) n-type switching operations with $V_d$ = 50 mV and different back gate voltages for a single Si-NW SB-TFTs with L = 16 $\mu$m, having an additional back-side gate to control the polarity where a voltage of $V_{gb}$ is applied. The corresponding band diagrams for p-type and n-type operations are shown in (c) and (d), respectively. (e) Schematic device structure of a device with top gate and an additional back gate.

where $R_{ch}$ and $R_{NiSi}$ are the resistance values of the active channel ($L_{ch} = 2\,\mu m$) and the $NiSi_2$, respectively. Therefore, the normalized $R_{ext\_eff}$ [$R_{ext\_eff}$ /$R_{ext\_eff}$ ($V_{gf} = -5$ V)] vs $V_{gf}$ as a function of the extension length was extracted by using a simple subtraction method (Fig. S3 in the supplementary material), and the result is shown in Fig. 4(b). $R_{ext\_eff}$ with short extension was continuously decreasing for increasing $|V_{gf}|$, while the external resistance with long extension seems to maintain a constant value regardless of $V_{gf}$. These behaviors are consistent with the simulated potential distributions from Fig. 3. Most of the Si-NW extension in the device with a short length is affected by $V_{gf}$, and the hole carrier concentration in the Si-NW extension region is increased by the E-field created from a negative $V_{gf}$. In addition, the probability of hole injection through the $NiSi_2$/Si-NW hetero-junction is raised by thinning the effective SB by the E-field created from $V_{gf}$. These results give rise to a reduction of $R_{ext\_eff}$ for higher $|V_{gf}|$ in the short length device.

*I–V* contour transport-maps of Si-NW SB-TFTs were obtained for different L values to understand easily the dominant conduction mechanism by varying $V_d$ as well as $V_{gf}$.[25,26,28] The *I–V* map of the device with $L = 4\,\mu m$ displayed a typical behavior of an ambipolar SB transistor as shown in Fig. 5(a).[25,28] The electron and the hole dominant conduction regime can be clearly distinguished by the dotted black line. The thermionic-emission (TE) and field-emission (FE) dominant conduction regimes can also be identified in the blue and red area of the *I–V* map, respectively. The activation energy ($E_{ac}$) map from the temperature dependent *I–V* map confirmed the conclusions from previous work.[28] For the device with a long $L = 16\,\mu m$, the *I–V* map showed only hole carrier dominant conduction in the whole bias-range as can be seen in Fig. 5(c). Interestingly, in the case of the device with intermediate $L = 6\,\mu m$, the drain-bias dependence of the electron dominant conduction can be observed in Fig. 5(b). A p-type transistor operation with negligible electron conduction was obtained when $|V_d|$ is small. However, as increasing $|V_d|$, the electron conduction was getting pronounced and an ambipolar transfer curve results at high $|V_d|$. This is most probably due to the enhanced electron injection from the source (when $V_d > 0$) or drain (when $V_d < 0$), induced by both $V_d$ and $V_{gf}$.

A clear reconfigurable operation was successfully demonstrated by applying a back-side gate voltage ($V_{gb}$, additional polarity gate) on a single physical device with $L = 16\,\mu m$, as shown in Fig. 6. The polarity of the switching characteristics can be tuned by controlling the effective SB width at the S/D sides using the $V_{gb}$, and $V_{gf}$ dominates the potential barrier and carrier concentration of the Si-NW below the gated channel area $L_{ch}$.[20,22] A negative $V_{gb}$ reduces the effective SB width for holes and increases the injection of holes through the thinned SB (p-type operation). The potential barrier created by the negative $V_{gb}$ completely suppresses the electron injection at the same time. In contrast, a positive $V_{gb}$ reinforces the electron injection through the thinned SB for electrons (n-type operation). The energy band diagrams as illustrated in Figs. 6(c) and 6(d) explain the unique operation mechanism of the polarity-controlled Si-NW SB-TFTs.

The $V_{gb}$ can also result in an electrostatic-doping of the Si-NW including the extension area. This introduces a variation of the series resistance ($R_{sd}$) and the threshold voltage ($V_{th}$) of the

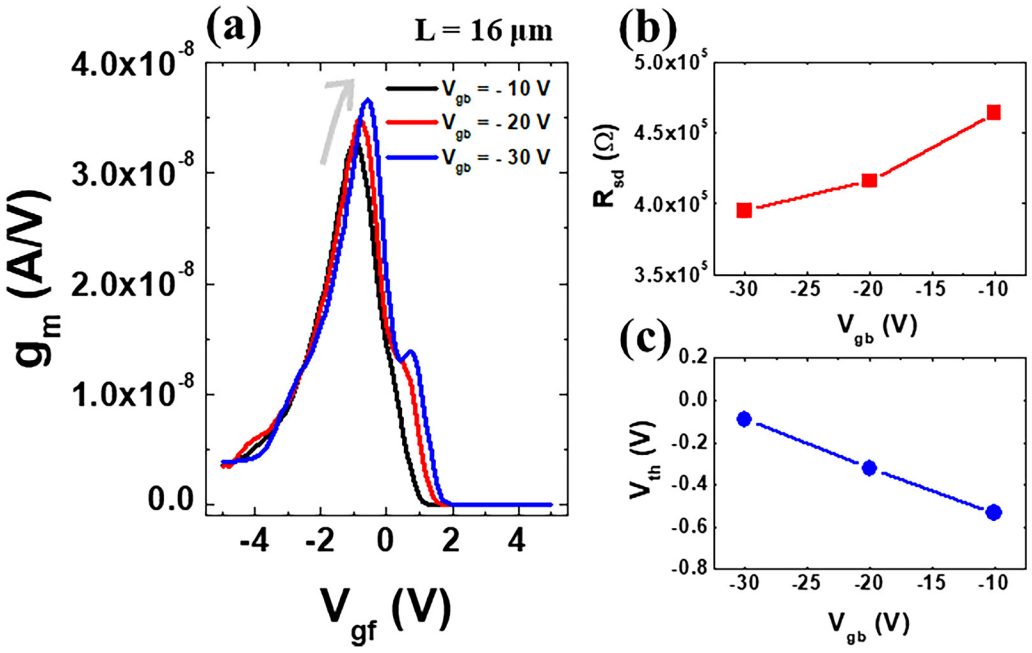


**FIG. 7.** (a) $V_{gb}$ dependent transconductance ($g_m$), (b) series resistance ($R_{sd}$), and (c) threshold voltage extracted by the Y-function method with varying $V_{gb}$ of the p-branch in the Si-NW SB-TFTs with $L = 16\,\mu m$.

Si-NW SB-TFTs. Figure 7(a) shows the $V_{gb}$ dependent transconductance ($g_m$) of the p-branch from Fig. 6(a). The maximum $g_m$ at the peak is related to the intrinsic carrier mobility in the devices.[29,30] For a decreasing $V_{gb}$ from −10 to −30 V, the $g_m$ value at the peak increased possibly due to a reduced $R_{sd}$ effect. Further decreasing $V_{gb}$ accumulates more holes in the extension regime and this decreases the resistance value of the extension which is a major part of $R_{sd}$. $R_{sd}$ can be estimated by using the Y-function method according to[31]

$$Y = \frac{I_d}{\sqrt{g_m}} = \sqrt{\beta V_d} \times (V_{gf} - V_{th}), \quad (1)$$

where β is the conductance gain. Linear slopes in the Y-function

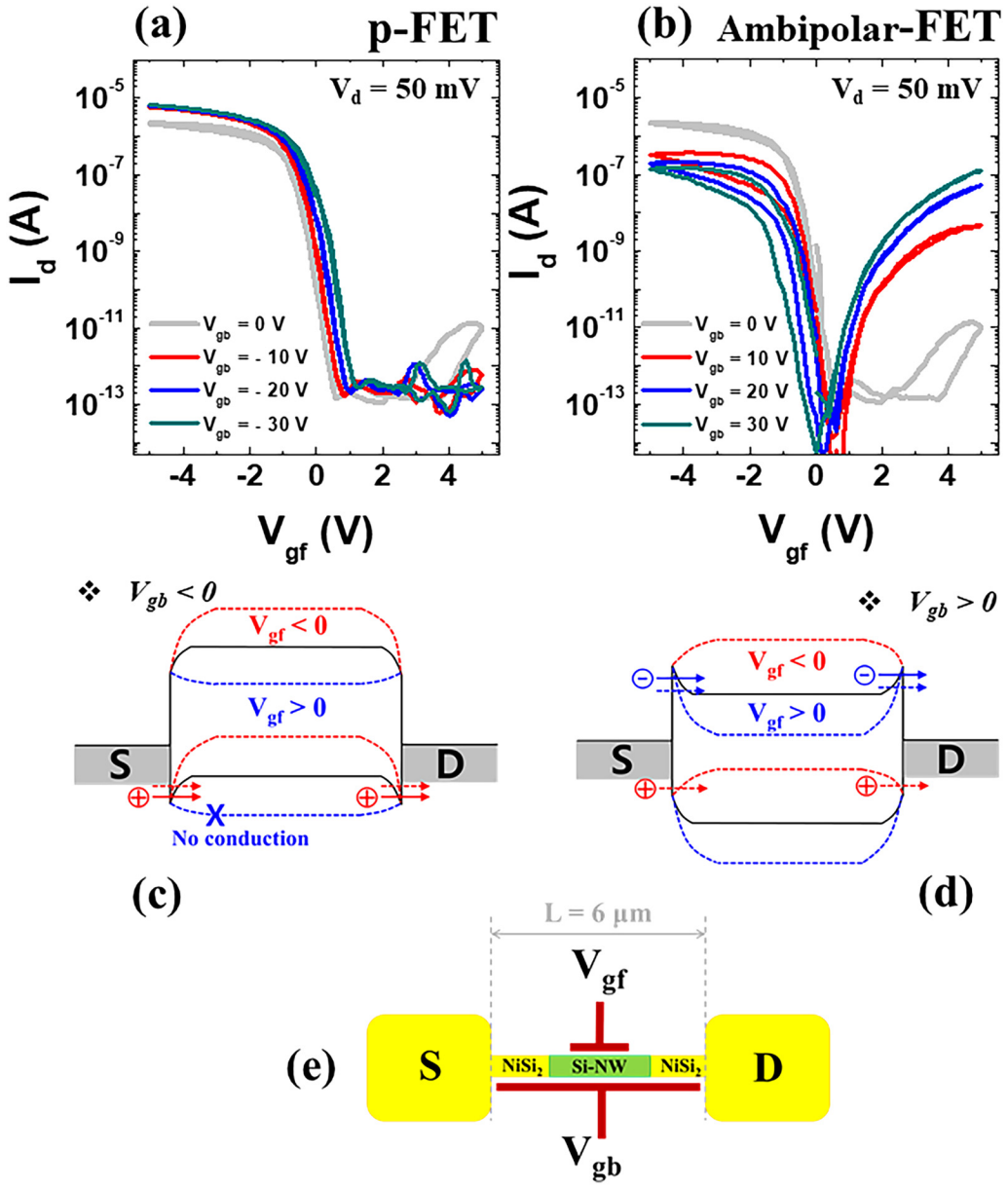


**FIG. 8.** Reconfigurable operation of the device with intermediate L = 6 $\mu$m with short extension. (a) Transfer characteristics p-type for different negative values of $V_{gb}$ and (b) transfer characteristics for different positive voltages of $V_{gb}$. For negative $V_{gb}$, p-type and for positive $V_{gb}$, ambipolar behavior are observed. The corresponding band diagrams for p-type and ambipolar operation are shown in (c) and (d), respectively. (e) A schematic device structure of a device with top gate and an additional back gate.

plot with varying $V_{gb}$ can be seen in Fig. S4 in the supplementary material. Then, the series resistance $R_{sd}$ was extracted from the following equation:

$$R_{sd} \approx \left(\frac{\beta V_d}{I_d} - \frac{1}{V_{gf} - V_{th}}\right)/\beta. \quad (2)$$

Indeed, the extracted $R_{sd}$ was reduced as decreasing $V_{gb}$ as shown in Fig. 7(b). The threshold voltage was also determined from the Y-function equation, and the $V_{th}$ increased as decreasing $V_{gb}$ in Fig. 7(c). More positive charges (hole carriers) in the Si-NW are initially accumulated when further decreasing $V_{gb}$. These holes make it easier to reach the on-state of the device at a lower $|V_{gf}|$.

Figure 8 finally shows the $V_{gb}$ induced reconfigurable operation of the device with an intermediate $L = 6\,\mu m$ having a short extension. Although the effective SB width at the S/D is influenced by both $V_{gf}$ and $V_{gb}$ in the device, a perfect p-type switching operation was exhibited in Fig. 8(a) when $V_{gb}$ is negative. However, ambipolar characteristics were observed in Fig. 8(b) for positive $V_{gb}$ since the injection probability for both electrons and holes through the SB is modulated by $V_{gf}$ at positive $V_{gb}$. The asymmetric drain current behavior at the same absolute $|V_{gb}|$ between p-FET and ambipolar-FET is due to different values of the initial SB height for electrons and holes at the $NiSi_2$/Si junctions. Moreover, a negligible $V_{gb}$ effect on the transfer curves is measured in the device with short $L = 4\,\mu m$, where the front-gate covers the whole SB junctions (Fig. S5 in the supplementary material). The results verified that the controllability of the front-gate ($V_{gf}$) was stronger than that of back-side gate ($V_{gb}$) due to the structural features surrounding the Si-NW by the front-gate and the thicker back gate dielectric.[32]

## CONCLUSIONS

In summary, reconfigurable SB-TFTs based on bottom-up grown Si-NWs have been fabricated, and their electrical performance and transport mechanism were investigated in detail for different device structures and a double gating effect. The Si-NW SB-TFTs with a long effective extension ($L_{ext\_eff}$) showed a p-type unipolar transfer curve and a degradation of $g_m$ at high $|V_{gf}|$, while an ambipolar-like behavior and continually increased $g_m$ even at high $|V_{gf}|$ were observed in the device with a short extension. The $NiSi_2$/Si-NW SB junction at the S/D sides was considerably affected by the E-field created by $V_{gf}$ in the short $L_{ext\_eff}$ device, and those were verified from the results obtained by numerical simulation and the $V_{gb}$ dependent $R_{ext\_eff}$. The device length dependent drain-bias effect was also clearly exhibited in the *I–V* transport-map of the Si-NW SB-TFTs. In addition, the reconfigurable operation of the Si-NW SB-TFTs with additional back gate voltage $V_{gb}$ (the so-called polarity gate) was significantly influenced by the extension length. Finally, the $V_{gb}$ induced electrostatic-doping effect on the reconfigurable operation of Si-NW SB-TFTs was also connected to the extracted key electrical parameters such as mobility, series resistance, and threshold voltage.

## SUPPLEMENTARY MATERIAL

See the supplementary material for transfer curve of fully silicided Si-NW, FlexPDE scripts, a simple subtraction method for $R_{ext\_eff}$ extraction, Y-function plots, and transfer curves of a short length device with varying $V_{gb}$.

## EXPERIMENTAL DETAILS

For this work, the Si-NW SB-TFTs were fabricated on highly doped Si (P + +)/$SiO_2$ (400 nm thick). The contact printing method was used for alignment of chemical vapor deposition (CVD) grown Si-NWs in a parallel array, and approximately 8 nm thick $SiO_2$ shell surrounding Si-NWs was formed by a rapid thermal annealing process (RTP). Ni electrodes with interdigitated shape were defined by a photo-lithography process for S/D formation. Then, Schottky-junction between $NiSi_2$ and Si-NW at S/D sides was created by the silicidation process under 500 °C for 30 s, and a 20 nm thick $Al_2O_3$ as gate insulator was deposited by using the atomic layer deposition (ALD) method. Further detail fabrication process and growth mechanism of Si-NWs were explained in previous papers.[15,25,33] *I–V* characteristics were obtained by using Keithley 4200 measurement unit, and FlexPDE software (PDE Solution, Inc.) was used for numerical simulations.[34] Many transfer curves were recorded by using the measurement system with varying $V_{gf}$ and $V_d$, and then *I–V* maps were obtained by converting as-measured data into a contour plot.[25]

## AUTHORS' CONTRIBUTIONS

D.-Y.J. and S.J.P. contributed equally to this work.

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## DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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