

# Polycrystalline Ge Nanosheets Embedded in Metal-Semiconductor Heterostructures Enabling Wafer-Scale 3D Integration of Ge Nanodevices with Self-Aligned Al Contacts

Masiar Sistani, Raphael Böckle, Lukas Wind, Kilian Eysin, Xavier Maeder, Peter Schweizer, Johann Michler, Alois Lugstein, and Walter M. Weber\*

The ability to stack nanosheet transistors is an important prerequisite for the realization of vertically monolithic 3D integrated circuits enabling higher integration densities of functions and novel circuit topologies that relax miniaturization constraints. In this respect, a wafer-scale platform is presented embedding high-quality nanoscale polycrystalline Ge channels into monolithic metal-semiconductor heterostructures. Thereto, a fabrication scheme comprising a combination of flash lamp annealing, crystallizing ultra-thin amorphous Ge nanosheets, and a thermally induced Al-Ge exchange reaction is demonstrated, facilitating the formation of self-aligned Al leads enabling sharp Al-Ge heterojunctions. The high quality of the obtained polycrystalline Al-Ge-Al heterostructure nanosheets is confirmed by  $\mu$ -Raman, scanning transmission electron microscopy, energy-dispersive X-ray spectroscopy, and electron backscatter diffraction measurements. Embedded in back- and top-gate field-effect transistor architectures, the electrical transport in polycrystalline Al-Ge-Al heterostructures is systematically analyzed. Enabling a complementary metal-oxide-semiconductor compatible wafer-scale accessibility of high-quality polycrystalline Ge with self-aligned Al contacts, the proposed platform significantly contributes to the development of a broad spectrum of emerging 3D integrated Ge nanodevices.

## 1. Introduction

Accompanied with the continuing miniaturization of modern field-effect transistor (FET) architectures, the physical distance between junctions has entered sub-10 nm dimensions,<sup>[1]</sup> which demands extraordinarily steep and reproducible doping concentration gradients at the junctions. However, due to dopant diffusion and the statistical nature of the distribution of the doping atoms, the fabrication of ever-smaller reproducible junctions gets increasingly challenging. At the same time, emerging distributed computing paradigms are placing extraordinary demands on hardware performance and efficiency, which is forcing a shift of research efforts towards the integration of new materials as well as the exploration of tailored device and circuit architectures.<sup>[2–4]</sup> In this respect, low-dimensional Ge structures,<sup>[4–6]</sup> have gained significant attention, due to their superior electrical properties compared to conventional Si devices.<sup>[7,8]</sup> Although crystalline Ge films can be obtained through

wafer bonding to achieve Ge on insulator substrates,<sup>[9]</sup> epitaxial overgrowth,<sup>[10]</sup> or the membrane transfer method,<sup>[11]</sup> each of these methods has its limitations. While the wafer bonding method is expensive and requires a complex thinning of the Ge layer, the epitaxial growth needs very thick buffer layers and the membrane transfer method is not applicable on wafer-scale.<sup>[5]</sup> In this respect, the combination of dedicated deposition and crystallization methods has already been shown to deliver polycrystalline semiconductor layers of high electronic quality.<sup>[12]</sup> Without being explicitly limited to a Si/SiO<sub>2</sub> substrate, solid-phase crystallization (SPC) and flash lamp annealing (FLA) processes are principally compatible with system-on-glass<sup>[13–15]</sup> or flexible electronics<sup>[16–18]</sup> for example, mobile electronic components, such as high-resolution displays, radio-frequency identification components, logic or memory circuits. Nonetheless, to exploit the full potential of nanoscale Ge structures, high quality electrical contacts are of utmost importance towards the integration of reliable future ultra-scaled devices. In this respect, emerging concepts

Dr. M. Sistani, R. Böckle, L. Wind, K. Eysin, Dr. A. Lugstein,  
Prof. W. M. Weber  
Institute of Solid State Electronics  
TU Wien  
Vienna 1040, Austria  
E-mail: walter.weber@tuwien.ac.at

Dr. X. Maeder, Dr. P. Schweizer, Dr. J. Michler  
Swiss Federal Laboratories for Materials Science and Technology  
Laboratory for Mechanics of Materials and Nanostructures  
Thun 3602, Switzerland

 The ORCID identification number(s) for the author(s) of this article can be found under <https://doi.org/10.1002/aelm.202100101>.

© 2021 The Authors. Advanced Electronic Materials published by Wiley-VCH GmbH. This is an open access article under the terms of the Creative Commons Attribution License, which permits use, distribution and reproduction in any medium, provided the original work is properly cited.

DOI: 10.1002/aelm.202100101

like self-aligned germanide<sup>[19]</sup> contacts and pure metal-semiconductor junctions like Al-Ge heterostructures<sup>[20,21]</sup> were developed. As scaling limitations of the gate length affect these devices likewise to metal-oxide-semiconductor (MOS) FETs, the stacking of such high-speed low-power thin-film transistors on interlayer dielectrics is attractive for the realization of vertically monolithic 3D integrated circuits with higher functional integration relaxing sizing constraints of the individual semiconductor devices.<sup>[22,23]</sup>

## 2. Results and Discussion

In this paper, we present a wafer-scale approach to achieve polycrystalline Ge nanosheets crystallized by FLA embedded in monolithic Al-Ge-Al heterostructures as formed via a thermally induced Al-Ge exchange reaction. **Figure 1a** shows exemplarily the fabrication scheme for an individual polycrystalline Al-Ge-Al heterostructure device. However, without restrictions, this technique enables the parallel processing of arrays of structures of different geometry on a wafer-scale. First, nanosheets are patterned onto a highly p-doped Si wafer using electron beam lithography (EBL), evaporation of 2 to 50 nm thin amorphous Ge, and lift-off techniques. Next, plasma-enhanced chemical vapor deposition (PECVD) is used to deposit a SiO<sub>2</sub> capping layer before FLA is applied to initiate the crystallization of the amorphous Ge nanosheets. Al contact pads are fabricated by optical lithography, native oxide removal, sputter deposition, and lift-off techniques. Finally, the actual heterostructure formation is induced by rapid thermal annealing (RTA) at a temperature of  $T = 624$  K in forming gas atmosphere.

**Figure 1b** shows SEM images of Ge structures with different widths ( $W$ ) of the Ge pattern contacted by Al pads after RTA. The images reveal dark segments emerging from the contacts, which prolonged along the Ge structures during RTA. Overlaying the SEM image of the upper left nanosheet heterostructure with its energy-dispersive X-ray spectroscopy (EDX) map confirms an Al-Ge-Al structure comprising Al contacts connecting a Ge segment of length  $L$ . Additional EDX maps of Al-Ge-Al heterostructure nanosheets with different width are shown in **Figure S1**, Supporting Information.

To achieve short Ge channels, we use consecutive annealing steps, accompanied by ex situ SEM imaging. **Figure 1c** shows SEM images of a typical annealing sequence, finally resulting in a 100 nm long Ge channel embedded in a monolithic polycrystalline Al-Ge-Al heterostructure. To demonstrate that the proposed heterostructure formation process enables the formation of short Ge channels embedded in Al-Ge-Al heterostructures with abrupt Al-Ge junctions, **Figure S2**, Supporting Information shows a SEM image of a heterostructure nanosheet with a width of  $W = 50$  nm, a height of  $h = 25$  nm and a metal-lurgic Ge channel length of  $L = 40$  nm.

To prove the crystallinity of the Ge segment embedded in the Al-Ge-Al heterostructure, a cross-sectional scanning transmission electron microscopy (STEM) at one of the Al-Ge interfaces of a 1  $\mu\text{m}$  wide, 25 nm thick and 1.5  $\mu\text{m}$  long Ge segment was conducted (**Figure 2a**). The enlarged view shows a close-up high-angle annular dark-field (HAADF) STEM image of the Al-Ge junction. **Figure 2b** shows an EDX line-scan revealing a sharp Al-Ge interface. The grain-size of the Ge segment with

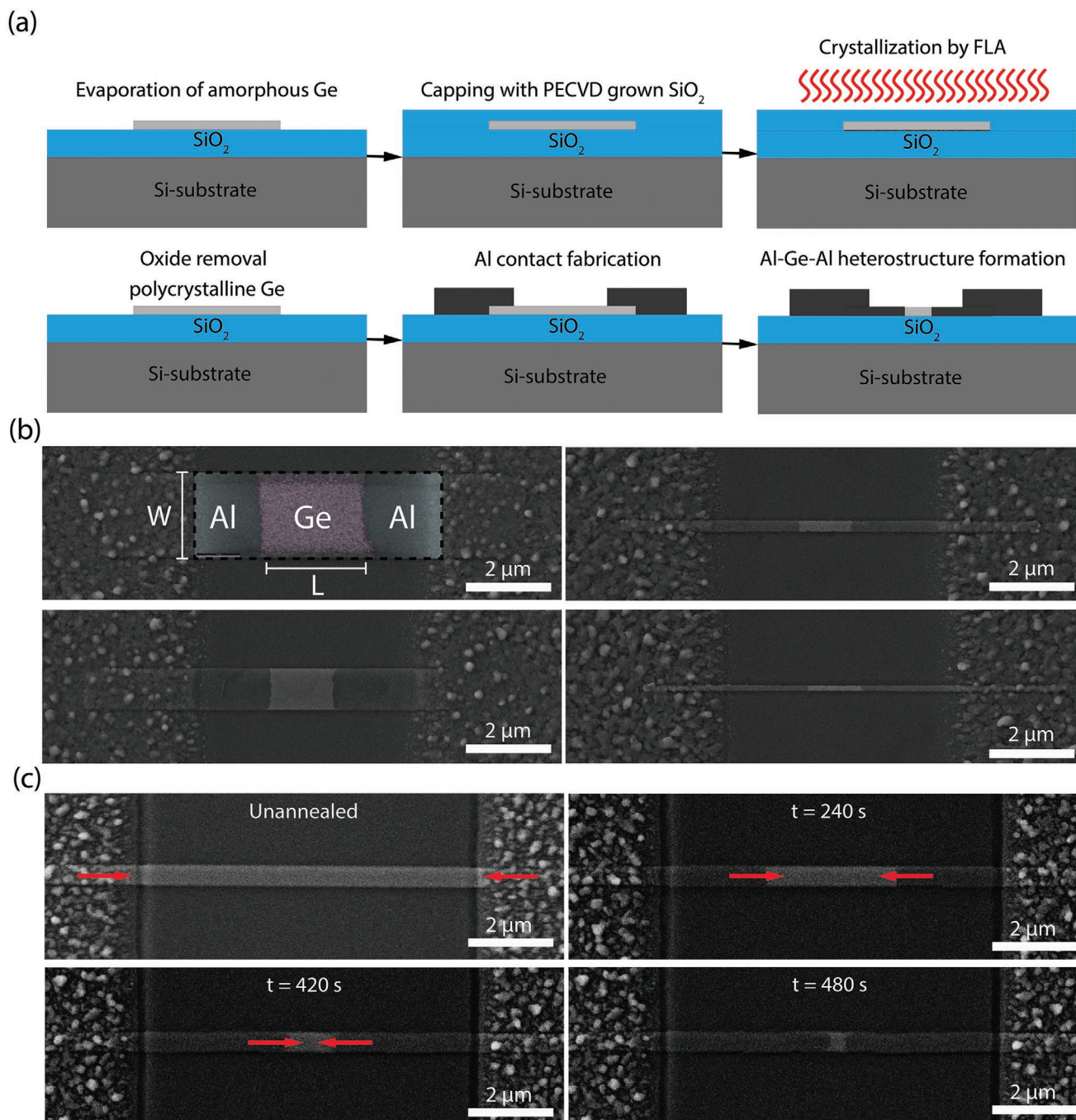
$h = 25$  nm is  $\approx 20$  nm  $\times$  20 nm (**Figure S3**, Supporting Information). This is in agreement with studies on polycrystalline Ge layers formed by SPC, showing that the grain size dramatically decreases for thinner structures.<sup>[22]</sup>

Further, **Figure 2c** shows a comparison of the normalized  $\mu$ -Raman spectrum of an amorphous (black) and different Ge nanosheets flashed with energies between  $E = 60$  and 90 J cm<sup>-2</sup> (maximum energy of the FLA system). While the amorphous Ge nanosheet shows a broad peak, signs of crystallization are observable for FLA Ge nanosheets with the peak becoming sharper and more symmetric for increased FLA energies. The  $\mu$ -Raman spectra of the FLA Ge nanosheet reveal a distinct peak assigned to the Stokes transverse optical (TO) modes of Ge at  $\approx 301$  cm<sup>-1</sup>.<sup>[24-26]</sup>

For benchmarking, **Figure S4**, Supporting Information compares the  $\mu$ -Raman spectra of our polycrystalline Ge nanosheets obtained by FLA, with ones that we have crystallized using a more common SPC procedure ( $T = 773$  K for  $t = 10$  h in N<sub>2</sub> atmosphere).<sup>[13]</sup> Indicating a higher quality polycrystalline Ge, a much narrower Ge TO mode was found for the FLA based polycrystalline Ge nanosheets ( $E = 90$  J cm<sup>-2</sup>). Further, the successful FLA crystallization approach is advantageous to enable an overstacking of functional polycrystalline Ge layers in a CMOS fabrication environment, as only the surface is highly heated without substantially altering the substrate temperature. An example for such a process flow is supplied in the supporting information. Further, one of the key advantages of the FLA process is its ultrashort heating time, which prohibits significant dopant diffusion commonly observed for SPC. In particular, intermixing and diffusion in the proposed device fabrication scheme are further excluded by the encapsulation of the amorphous Ge nanosheets by SiO<sub>2</sub>.

Further, **Figure 2d** reveals that the full width at half maximum (FWHM) of the Ge mode approaches the bulk value of crystalline Ge ( $\Gamma = 3.4$  cm<sup>-1</sup>).<sup>[27]</sup> which indicates a higher degree of crystallinity by increasing the applied FLA energy.<sup>[28]</sup> Moreover, in agreement with quantum confinement, **Figure 2e** reveals that a thinner polycrystalline Ge results in a down-shift of the Ge TO mode.<sup>[29]</sup>

To investigate the electrical transport properties of our polycrystalline Al-Ge-Al heterostructures, **Figure 3a** shows the resistivity calculated from temperature-dependent  $I/V$  measurements as a function of temperature in the range between  $T = 77.5$  and 400 K compared to a polycrystalline Al nanosheet. Two-terminal measurements were conducted, given the intruding nature of the Al contacts that hinders the validity of four-probe measurements. The extracted resistivity includes a series resistance originating from the polycrystalline Al leads of the heterostructure, as well as the one related to the expected Schottky junctions. To determine the influence of this series resistance, the resistivity of a fully transformed polycrystalline Al nanosheet with a width of  $W = 2$   $\mu\text{m}$ , a height of  $h = 5$  nm, and a length of  $L_{\text{Al}} = 3.3$   $\mu\text{m}$  was evaluated. Based on these investigations, a resistivity  $\rho = 100 \times 10^{-9}$   $\Omega\text{m}$  was calculated, which is  $\approx 7.5$  times larger than the bulk value of Al.<sup>[30]</sup> This might be related to an increased influence of surface scattering in nanostructures<sup>[31]</sup> as well as to the size-effect of polycrystalline interconnects given by the contribution of scattering at crystallite grain boundaries as observed in Cu nano-interconnects<sup>[32]</sup> or due to current crowding at the

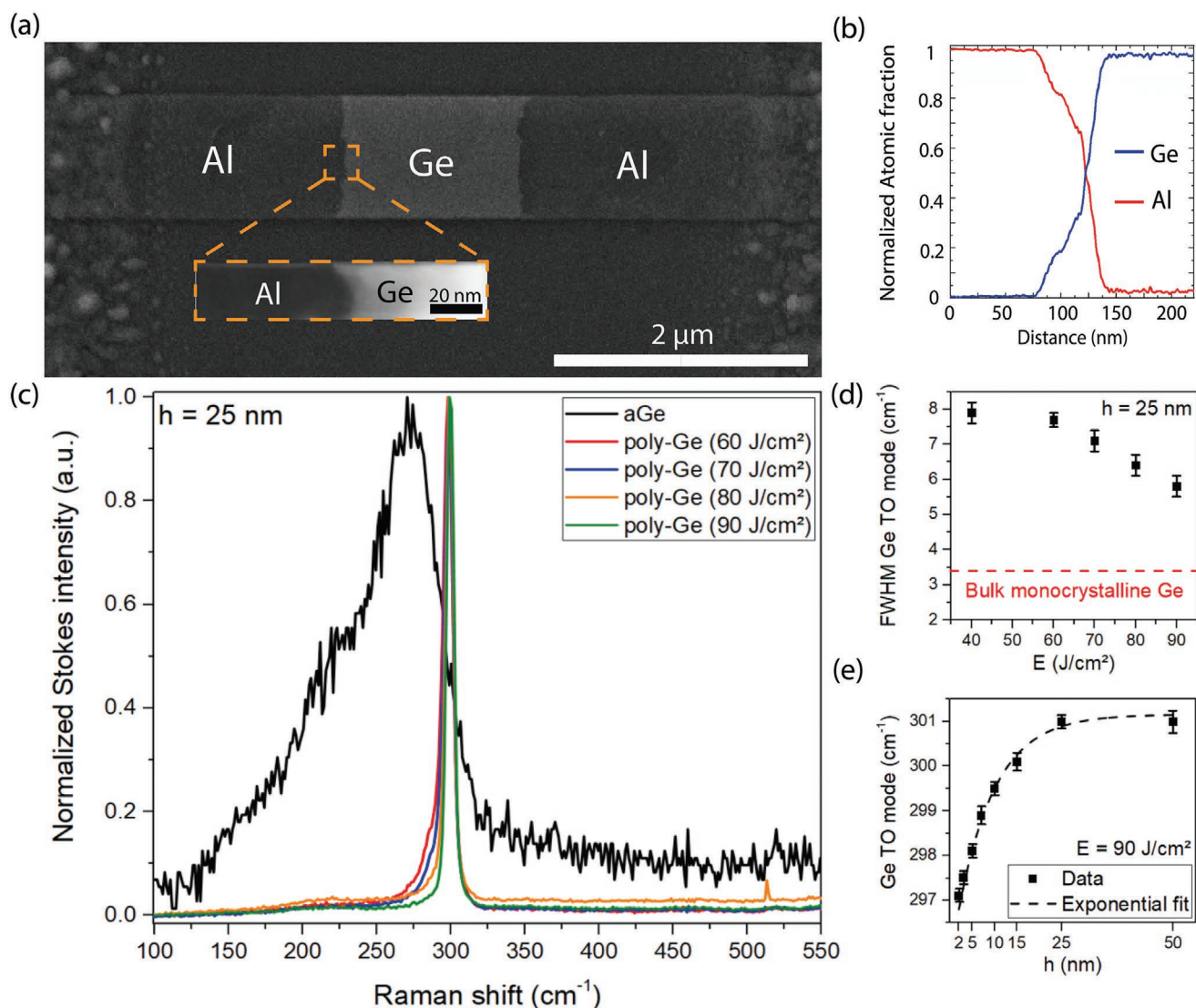


**Figure 1.** a) Processing scheme for the wafer-scale fabrication of Al-Ge-Al heterostructures, b) SEM images of Al-Ge-Al heterostructures with different Ge channel widths and lengths. Overlaying the SEM image of the upper left nanosheet heterostructure with its EDX map confirms an Al-Ge-Al architecture after thermal annealing at  $T = 624$  K. c) Sequence of SEM images showing the annealing progress of an Al-Ge-Al heterostructure. The respective process times for annealing at  $T = 624$  K are indicated.

Al-lead/Al nanosheet interface as seen in metallic nanocrystalline carbon vias.<sup>[33]</sup> Upon cooling, the resistivity of the polycrystalline Al nanosheet is decreasing, which is associated with a decrease of phonon scattering at lower temperatures and is typical for metals.<sup>[34]</sup> As the resistance of an Al nanosheet is approximately six orders of magnitude smaller compared to polycrystalline Al-Ge-Al heterostructures, the

parasitic resistance of the Al leads to the Ge channel is in our case negligible.

Indicating diffusive transport, the resistivity of the polycrystalline Al-Ge-Al devices reveals a distinct temperature dependency. In such long Ge channels, the device resistance originates from scattering with phonons, crystal defects, and impurities.<sup>[35]</sup> While, upon cool-down to  $T = 200$  K, a gradual increase of resistivity was

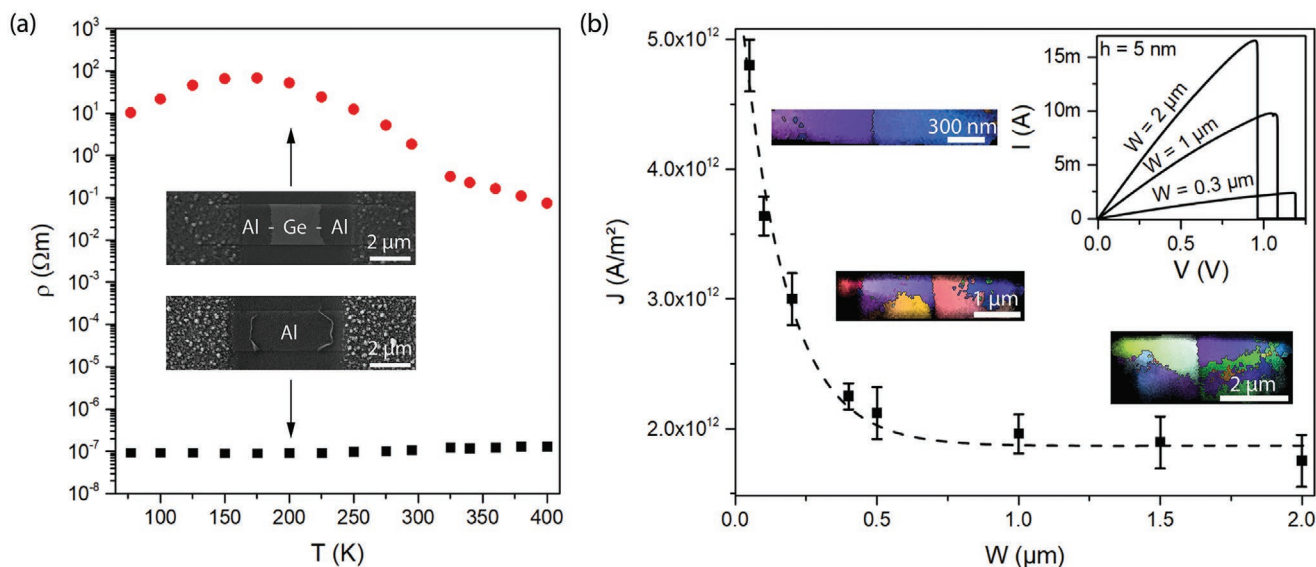


**Figure 2.** a) SEM image of an Al-Ge-Al heterostructure nanosheet. The inset is showing a cross-sectional HADF STEM image of the Al-Ge junction. b) EDX line-scan across the Al-Ge interface. c) Normalized  $\mu$ -Raman spectra of polycrystalline FLA Ge nanosheets for applying pulse energies between  $E = 60$  and  $90 \text{ J cm}^{-2}$  compared with an amorphous Ge nanosheet. All nanosheets have a height of  $h = 25 \text{ nm}$ . d) Comparison of the FWHM of the Ge TO mode depending on the applied FLA energy. The red dotted line denotes the FWHM of bulk monocrystalline Ge. e) Position of the Raman Ge TO mode depending on the height of the Ge nanosheets. The FLA pulse energy was set to  $E = 90 \text{ J cm}^{-2}$ .

measured, below this temperature, the resistivity appeared to decrease again. As polycrystalline Ge nanostructures obtained by FLA are known to be naturally p-type,<sup>[36]</sup> we associate this effect to the extrinsic nature of the material, which exhibits a relatively constant carrier concentration and a significant mobility increase in this temperature regime.<sup>[37,38]</sup>

To investigate the quality of our polycrystalline Al nanosheets, we determined the current-carrying capacity by gradually increasing the current through the nanosheets in a two-terminal configuration while monitoring the voltage across the device. The inset of Figure 3b shows exemplary  $I/V$  characteristics recorded for three polycrystalline Al nanosheets with widths of  $W = 2, 1,$  and  $0.3 \mu\text{m}$ . The step-like decrease of the current indicates the breakdown of the nanosheet. For all investigated Al nanosheets, the slope of the  $I/V$  curve, that is, the resistance,

increased right before the point of failure, which is an indication of effective Joule heating ultimately leading to a melting induced failure.<sup>[39]</sup> Calculating the maximum current density ( $J_{\text{max}}$ ) leads to the remarkable result, that narrower nanosheets reveal a significantly higher failure current density compared to wider ones, with a peak value of  $J_{\text{max}} = 4.8 \times 10^{12} \text{ A m}^{-2}$  for a width of  $W = 100 \text{ nm}$ . Such exceptional ampacity values of thin metallic nanostructures were also observed for Au NWs<sup>[40,41]</sup> and Cu NWs<sup>[39]</sup> and are attributed to the combination of efficient heat dissipation due to the high surface-to-volume ratio and the high quality of the polycrystalline Al nanosheets.<sup>[39]</sup> Thus, to investigate the crystal structure and interface morphology of the formed Al-Ge heterostructures in more detail, we performed an electron backscatter diffraction (EBSD) analysis. The insets of Figure 3b show the EBSD maps of representative structures with widths between



**Figure 3.** a) Temperature dependence of the resistivity of a 5 nm thick polycrystalline Al-Ge-Al heterostructure device (red) and polycrystalline Al nanosheet (black). b) Current density of Al nanosheets with a height of  $h = 5$  nm depending on the width  $W$ . A selection of EBSD maps of Al devices with different  $W$  are inserted. The inset shows  $I/V$  characteristics of Al nanosheets with different  $W$  in a two-point configuration. A sudden step-like decrease of the current denotes the failure of the Al nanosheet.

$W = 2 \mu\text{m}$  and  $300 \text{ nm}$ . For wider structures, the Al contacts appeared to be polycrystalline with grain sizes in the  $\mu\text{m}$  range. For narrower structures, the number of grains decreases. Thus, for structures with widths below  $W = 400 \text{ nm}$  and Al contacts on both sides, long annealing times result in a full transformation of the Ge nanosheets in pure Al consisting of only two monocrystalline segments. Commonly observed, deposited Al contacts are known to show strong electromigration.<sup>[42]</sup> However, as Al nanosheets with  $W < 400 \text{ nm}$  fabricated from Al-Ge exchange show only two grains (one growing from each side) and reveal significantly higher  $J_{\text{max}}$  compared to wider structures, electromigration could be strongly diminished. In this respect, reliability tests of monocrystalline Al nanowires fabricated by Al-Ge exchange have shown a long-term stability exceeding the maximum current densities of bulk Al.<sup>[43]</sup> Despite the advantages of our monocrystalline Al contacts, we want to note that the use of our Al material should be restricted to the intimate metal/semiconductor contact, and that conventional, for example, Cu materials shall be used for the remaining interconnects.

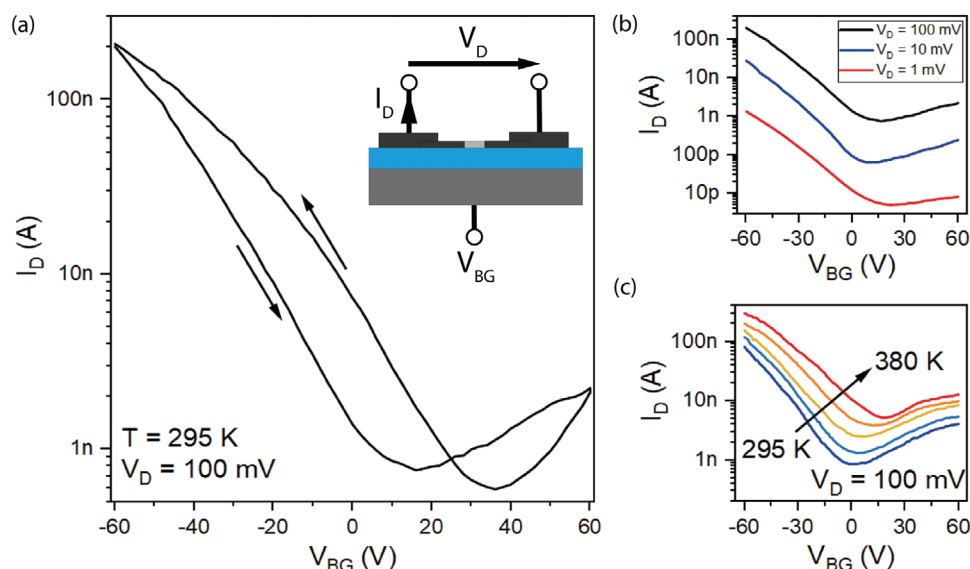
Importantly, for Al-Ge-Al devices with  $W < 400 \text{ nm}$ , we have also noticed a flatter and sharper Al-Ge interface (see Figure 1b and Figure S2, Supporting Information).

Next, transfer characteristic measurements were conducted to determine the modulation capability of the charge-carrier type and concentration in the Ge channel using the p-doped Si substrate as a common back-gate. The upper inset of Figure 4a provides a schematic illustration of the device architecture and the respective biasing. The main plot of Figure 4a shows the typical transfer characteristic of a FET device with a 5 nm thick Ge channel and a length of  $L = 100 \text{ nm}$  recorded with a gate voltage sweeping rate of  $0.25 \text{ V s}^{-1}$  at  $T = 295 \text{ K}$ .

Biasing with  $V_D = 1, 10, \text{ and } 100 \text{ mV}$  (Figure 4b), the device exhibits a weak ambipolar transfer characteristic, with hole accumulation for  $V_G < 20 \text{ V}$  and moderate inversion for

$V_G > 40 \text{ V}$ . Figure S8, Supporting Information shows a contour plot of an  $I/V$  measurement between  $V_D = -1$  to  $1 \text{ V}$  for sweeping the back-gate voltages between  $V_{\text{BG}} = -40$  and  $40 \text{ V}$ . At  $V_D = 1 \text{ V}$  peak current densities of  $J_h = 1.5 \times 10^8 \text{ A m}^{-2}$  (holes) and  $J_e = 2 \times 10^6 \text{ A m}^{-2}$  (electrons) were calculated.

Further, we observed a pronounced hysteresis not only dependent on  $V_{\text{BG}}$ , but also the gate voltage sweeping direction. This behavior should be related to the commonly observed surface-doping<sup>[44,45]</sup> effect of Ge based nanodevices where acceptor-like traps shift the energy band structure throughout the Ge channel, causing the usual p-type behavior of nominally intrinsic Ge nanodevices.<sup>[44,46]</sup> Further, the transfer characteristic remarkably reveals that even applying low drain voltages down to  $V_D = 1 \text{ mV}$ , an  $I_{\text{ON}}/I_{\text{OFF}}$  ratio of  $\approx 10^2$  can be achieved. Assuming thermionic emission, the effective Schottky barrier height (SBH) for electrons of the Al-Ge junction can be obtained from the slope of the activation energy plot of  $\ln(J/T^2)$  versus  $1000/T$  at various bias voltages (see supporting information). The thereof calculated SBH in the sub-threshold region of electron-driven transport was estimated to be  $102 \pm 10 \text{ meV}$ . Further, as shown in Figure S9, Supporting Information, the overall resistance of the polycrystalline Al-Ge-Al heterostructure devices with a structural width of  $W = 2 \mu\text{m}$  is directly proportional to the Ge segment length corresponding to a resistivity of  $\rho = 2 \pm 1 \Omega\text{m}$ , which is almost a decade lower compared to similar devices without FLA treatment (see Figure S10, Supporting Information). We associate the dominant p-type conduction and the observed small effective Schottky barrier of our Al-Ge-Al heterostructure nanosheets to defects in the polycrystalline Ge channel providing shallow acceptor levels generating holes at room temperature, which is in agreement with previous studies.<sup>[47]</sup> Notably, this effect appeared to be more pronounced with increasing layer thickness as only negative effective Schottky barriers could be found for heterostructures with



**Figure 4.** a) Transfer characteristics of a polycrystalline Al-Ge-Al heterostructure nanosheet with  $W = 2 \mu\text{m}$ ,  $h = 5 \text{ nm}$ , and  $L = 100 \text{ nm}$  for bias voltages of  $V_D = 100 \text{ mV}$ . The arrows indicate the gate voltage sweeping direction. The inset is showing a schematic of the polycrystalline Al-Ge-Al heterostructure embedded in a common back-gated FET architecture. b) Comparison of transfer characteristics recorded for  $V_D = 1, 10,$  and  $100 \text{ mV}$ . The measurements were conducted at ambient conditions. c) Temperature dependence of the transfer characteristics for a bias voltage of  $V_D = 100 \text{ mV}$ .

a sheet height of  $h = 25 \text{ nm}$ , indicating a barrier thin enough for tunneling resulting in a quasi-ohmic contact.<sup>[48]</sup>

Figure 4c shows the temperature dependence of the transfer characteristic for  $V_D = 100 \text{ mV}$  between  $T = 295$  and  $380 \text{ K}$ , indicating a positive variation with increasing temperature. As expected from theory, the characteristic flattens and an increase of the OFF-current with temperature is evident, which can be attributed to thermally generated carriers.<sup>[12,35]</sup> Nevertheless, ambipolar device operation can still be observed for all investigated temperatures.

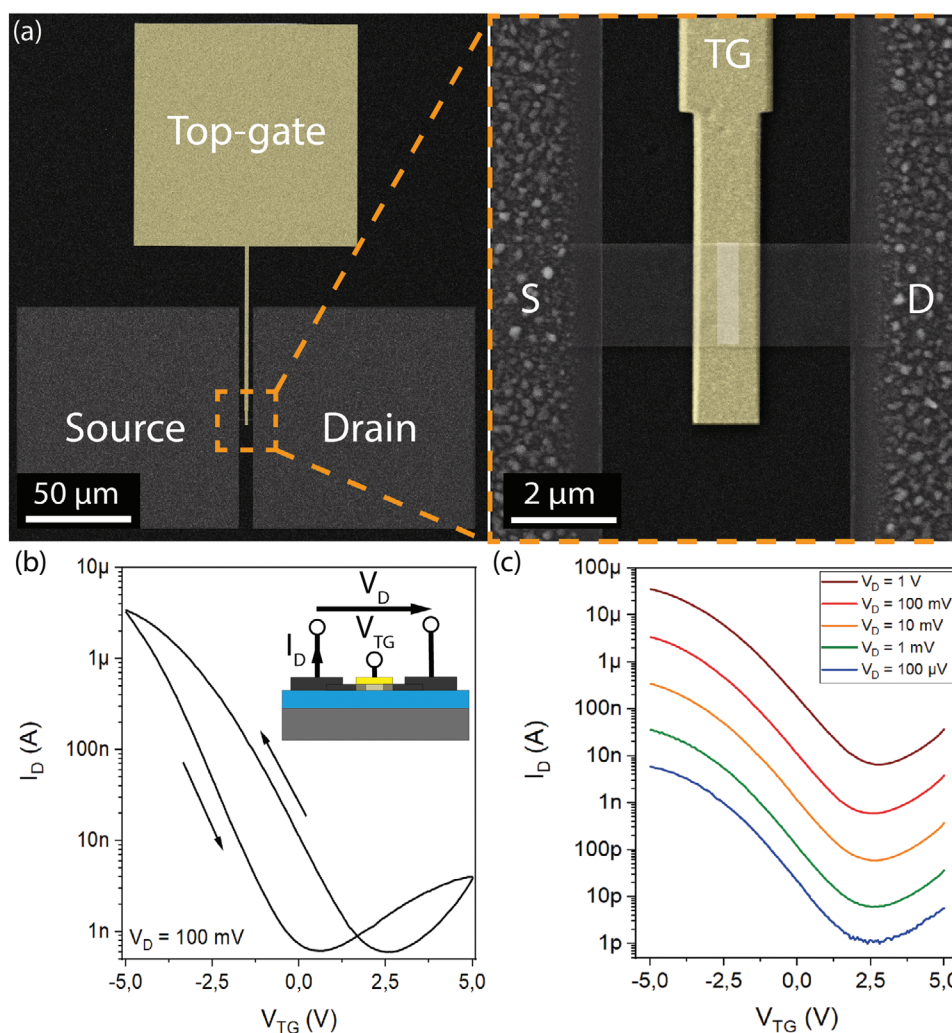
To improve the electrostatic control of the Ge channel and to decrease the absolute value of the applied gate voltage, an omega-shaped top-gate (TG) was fabricated. Thereto, the Al-Ge-Al heterostructure nanosheets were coated with a  $14 \text{ nm}$  thick  $\text{Al}_2\text{O}_3$  passivation grown by atomic layer deposition (ALD) and a source/drain (S/D) overlapping gate-contact was fabricated (see Figure 5a).

At this point, we want to note that although intrinsic Ge was used for device fabrication, negative surface charges accumulating in interband trap levels<sup>[44,49]</sup> contribute to an overall p-type behavior of the FET devices for both the bare as well as the  $\text{Al}_2\text{O}_3$  passivated Ge nanosheets. Further, as adsorbates influence the electrical behavior, it was mandatory to passivate the Ge channel prior to the Al-Ge heterostructure formation to reduce interface traps and surface disorder.<sup>[50]</sup> In agreement with previous reports,<sup>[51]</sup> using a high- $k$  passivation layer results in less pronounced hysteresis effects. However, according to Zhang et al.,<sup>[52]</sup> we assume that during the ALD process, a thin  $\text{GeO}_x$  layer is formed at the interface between the Ge nanosheet and the  $\text{Al}_2\text{O}_3$  passivation. Thereto advanced measures are required to reduce interface trap densities by the appropriate use of interlayer dielectrics. This could for instance include the removal/desorption of native  $\text{GeO}_x$  and the subsequent ordered stoichiometric thermal growth of

$\text{GeO}_2$  and/or posterior Ge oxy-nitride formation in order to reduce the level of interface states at the dielectric/germanium interface.<sup>[53]</sup>

Transfer characteristics of a polycrystalline Al-Ge-Al heterostructure nanosheet with  $W = 2 \mu\text{m}$ ,  $h = 5 \text{ nm}$ , and  $L = 300 \text{ nm}$  a bias voltage of  $V_D = 100 \text{ mV}$  are shown in Figure 5b. Similar to polycrystalline Al-Ge-Al heterostructure nanosheets in back-gate configuration, a hysteresis not only dependent on  $V_{TG}$ , but also the gate voltage sweeping direction and a slight ambipolar behavior was observed. Remarkably, as shown in Figure 5c, comparing the transfer characteristics recorded for bias voltages between  $V_D = 100 \mu\text{V}$  and  $1 \text{ V}$ , reveals that even applying ultra-low drain voltages down to  $V_D = 100 \mu\text{V}$ , an  $I_{ON}/I_{OFF}$  ratio of  $\approx 5 \times 10^4$  can be achieved. At  $V_D = 1 \text{ V}$ , we calculated peak current densities  $J_h = 3.6 \times 10^9 \text{ A m}^{-2}$  and  $J_e = 3.7 \times 10^6 \text{ A m}^{-2}$  (see Figure S11, Supporting Information). Compared to the back-gated device architecture, the current densities have improved by a factor of 24 and 1.8 respectively. Applying  $V_D = 100 \mu\text{V}$ , it was still possible to achieve  $J_h = 0.6 \times 10^5 \text{ A m}^{-2}$  and  $J_e = 5.7 \times 10^2 \text{ A m}^{-2}$ . For our top-gated (TG) devices an enhanced sub-threshold swing of  $SS = d[\log(I_D)]/dV_{TG} = 1.1 \pm 0.2 \text{ V}$  per decade was extracted. Figure S12, Supporting Information shows a contour plot of an  $I/V$  measurement between  $V_D = -1$  to  $1 \text{ V}$  for sweeping the TG voltages between  $V_{TG} = -5$  and  $5 \text{ V}$ .

As drain-induced barrier lowering (DIBL) could be a problem of small channel devices, advanced devices will have substantially thinner physical thicknesses of the gate dielectric. In the case of our polycrystalline Ge devices, the small bandgap comes on top in further deteriorating the off-state. However, our device platform is intended to be used to facilitate emerging device concepts such as reconfigurable FETs<sup>[8,54]</sup> with gate-electrodes covering the metal-semiconductor interfaces to change the device operation from an ambipolar characteristic to either a unipolar p- or n-type characteristic. As typical channel lengths



**Figure 5.** a) False color SEM images of a polycrystalline Al-Ge-Al heterostructure nanosheet integrated in a TG FET architecture with the position of the Ge channel being indicated in white. b) Transfer characteristics of a polycrystalline Al-Ge-Al heterostructure nanosheet with  $W = 2 \mu\text{m}$ ,  $h = 5 \text{ nm}$ , and  $L = 300 \text{ nm}$  for bias voltages of  $V_D = 100 \text{ mV}$ . The arrows indicate the gate voltage sweeping direction. The measurements were conducted at ambient conditions. The inset is showing a schematic of the polycrystalline Al-Ge-Al heterostructure embedded in a TG FET architecture. c) Comparison of transfer characteristics recorded for  $V_D = 100 \mu\text{V}$  to  $1 \text{ V}$ .

of such devices are in the order of  $L = 2 \mu\text{m}$ , DIBL should be strongly reduced and S/D leakage suppressed.

The performed systematic investigation of polycrystalline Al-Ge-Al heterostructure nanosheets embedded in back- and TG FET architectures confirmed their quality and revealed their high potential as a wafer-scale platform for the cost-efficient implementation of novel electronic devices and may pave the way for an unprecedented realization of circuits comprising stacked ultra-thin-body Ge FETs for 3D large-scale integration.

### 3. Conclusion

In conclusion, combining fully CMOS compatible Ge evaporation, FLA crystallization, and RTA annealing techniques, we explored a platform enabling a wafer-scale approach for the formation of nanoscale polycrystalline Ge nanosheets

monolithically embedded in a metal-semiconductor architecture comprising self-aligned Al contacts and sharp Al-Ge heterojunctions enabling source/drain overlapping gate-contacts. A structural analysis of the obtained polycrystalline Al-Ge-Al heterostructure nanosheets was confirmed by  $\mu$ -Raman, EDX, and EBSD measurements. Embedded in back- and TG FET architectures, the electrical transport properties of the proposed polycrystalline Al-Ge-Al heterojunctions were systematically probed and analyzed. We associate the p-type conduction and the observed small effective Schottky barrier of only  $102 \pm 10 \text{ meV}$  to defects in the polycrystalline Ge channel providing shallow acceptor levels. At  $V_D = 1 \text{ V}$ , we calculated peak current densities of  $J_h = 3.6 \times 10^9 \text{ A m}^{-2}$  and  $J_e = 3.7 \times 10^6 \text{ A m}^{-2}$ . Remarkably, even applying ultra-low drain voltages down to  $V_D = 100 \mu\text{V}$ , an  $I_{\text{ON}}/I_{\text{OFF}}$  ratio of  $10^4$  can be achieved. Further, the Al nanosheets connecting the Ge channel withstand remarkably high current densities of up to  $5 \times 10^{12} \text{ A m}^{-2}$ ,

important for their application as interconnects. Most notably, enabling a wafer-scale accessibility of nanoscale polycrystalline Ge with self-aligned Al contacts, the proposed architecture is perfectly suited for emerging device platforms such as stacked 3D integrated circuits, system-on-glass, or flexible electronics.

## 4. Experimental Section

**Device Fabrication:** Amorphous Ge nanosheets with adjustable layer thicknesses between  $h = 2$  and 50 nm were grown onto a 100 nm thick thermally grown SiO<sub>2</sub> layer atop of a 500 μm thick highly p-doped Si substrate. Thereto, a combination of EBL, electron beam assisted evaporation (10 kV, base pressure  $2.5 \times 10^{-8}$  mbar, intrinsic Ge with 99.999% purity), and lift-off techniques were used. The amorphous Ge structures were capped with 100 nm of PECVD grown SiO<sub>2</sub> deposited at  $T = 573$  K in order to provide a protective layer. Crystallization of the amorphous Ge structures was achieved by FLA at a pre-heat temperature of  $T = 473$  K in Ar atmosphere and pulse energies between  $E = 40$  and  $90$  J cm<sup>-2</sup> for  $t = 20$  ms. The SiO<sub>2</sub> capping layer was etched using a buffered HF (7:1) dip for 30 s. The polycrystalline Ge nanosheets were posteriorly contacted by Al pads fabricated by optical lithography, 125 nm Al sputter deposition, and lift-off techniques. A successive thermally induced exchange reaction by RTA at a temperature of  $T = 624$  K in forming gas (10% H<sub>2</sub>, 90% N<sub>2</sub>) atmosphere initiated the substitution of Ge by Al in accordance with the reactions involving single crystal Ge.<sup>[20,21]</sup> Facilitating this heterostructure formation scheme allows the integration of polycrystalline Al-Ge-Al heterostructures with tunable metallurgic channel lengths in a back-gated FET architecture using p-doped Si substrate as a common back-gate. Further, omega-shaped Ti/Au TGs were fabricated atop Al-Ge-Al heterostructure nanosheets coated with 14 nm of Al<sub>2</sub>O<sub>3</sub> as gate insulator deposited by ALD, using a combination of EBL, Ti/Au evaporation (7 nm Ti, 100 nm Au), and lift-off techniques.

**EDX and EBSD Measurements:** To prevent drift due to charging effects, the samples had been coated with 2 nm of carbon prior to EDX and EBSD mapping. EDX and EBSD were performed in a Tescan MIRA SEM using a Digiview 5 camera from EDAX (UK), with beam conditions of 20 kV and 5 nA. A step size of 50 nm had been used for the mapping.

**TEM Measurements:** TEM lamella preparation was performed using a Tescan Lyra FIB/SEM. The TEM images were acquired using a Thermo Fisher Scientific Titan Themis 200 G3 outfitted with a SuperX detector used for the EDX maps.

**μ-Raman Characterization:** A confocal multi-functional microscope setup (Alpha300, WITec) equipped with a frequency doubled Nd:YAG laser emitting linearly polarized light at  $\lambda = 532$  nm was used. For confocal μ-Raman measurements, a setup in backscattering geometry with a grating monochromator and a CCD camera (DV401- BV, Andor) was employed. An achromatic Nikon EPI EPlan 100× objective ( $NA = 0.9$ ,  $WD = 0.23$  mm), enabling a diffraction limited spot size of  $\approx 720$  nm was used.

**Electrical Characterization:** The electrical measurements were carried out at room temperature and ambient conditions using a combination of a semiconductor analyzer (HP 4156B) and a probe station. To minimize the influence of ambient light as well as electromagnetic fields, the probe station was placed in a shielded dark box. Temperature-dependent measurements (80–380 K) were performed in vacuum at a background pressure of  $\approx 5 \times 10^{-6}$  mbar using a cryogenic probe station (LakeShore PS-100) and a semiconductor analyzer (Keysight B1500A).

## Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

## Acknowledgements

M.S. and L.W. performed the device fabrication. M.S., R.B., and K.E. conducted the electrical measurements. M.S. carried out the μ-Raman characterization. X.M., P.S., and J.M. performed the STEM, EDX, and EBSD measurements and analysis. A.L. commented on the manuscript and provided helpful feedback. M.S. and W.M.W. conceived the project and contributed essentially to the experimental design. All authors analyzed the results and agreed on the manuscript. The authors gratefully acknowledge financial support by the Austrian Science Fund (FWF): project No.: P29729-N27. The authors further thank the Center for Micro- and Nanostructures for providing the cleanroom facilities.

## Conflict of Interest

The authors declare no conflict of interest.

## Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

## Keywords

3D integration, flash lamp annealing, metal–semiconductor heterostructures, nanosheets, polycrystalline germanium

Received: January 30, 2021

Revised: March 18, 2021

Published online: May 4, 2021

- [1] H. H. Radamson, H. Zhu, Z. Wu, X. He, H. Lin, J. Liu, J. Xiang, Z. Kong, W. Xiong, J. Li, H. Cui, J. Gao, H. Yang, Y. Du, B. Xu, B. Li, X. Zhao, J. Yu, Y. Dong, G. Wang, *Nanomaterials* **2020**, *10*, 1555.
- [2] C. Jia, Z. Lin, Y. Huang, X. Duan, *Chem. Rev.* **2019**, *119*, 9074.
- [3] P. Goley, M. Hudait, *Materials* **2014**, *7*, 2301.
- [4] W. M. Weber, T. Mikolajick, *Rep. Prog. Phys.* **2017**, *80*, 066502.
- [5] Z. Xia, H. Song, M. Kim, M. Zhou, T.-H. Chang, D. Liu, X. Yin, K. Xiong, H. Mi, X. Wang, F. Xia, Z. Yu, Z. (Jack) Ma, Q. Gan, *Sci. Adv.* **2017**, *3*, 1602783.
- [6] D. Wang, Y.-L. Chang, Q. Wang, J. Cao, D. B. Farmer, R. G. Gordon, H. Dai, *J. Am. Chem. Soc.* **2004**, *126*, 11602.
- [7] G. Gu, M. Burghard, G. T. Kim, G. S. Düsberg, P. W. Chiu, V. Krstic, S. Roth, W. Q. Han, *J. Appl. Phys.* **2001**, *90*, 5747.
- [8] A. Heinzig, S. Slesazek, F. Kreupl, T. Mikolajick, W. M. Weber, *Nano Lett.* **2012**, *12*, 119.
- [9] T. Akatsu, C. Deguet, L. Sanchez, F. Allibert, D. Rouchon, T. Signamarcheix, C. Richtarch, A. Boussagol, V. Loup, F. Mazen, J.-M. Hartmann, Y. Campidelli, L. Clavelier, F. Letertre, N. Kernevez, C. Mazure, *Mater. Sci. Semicond. Process.* **2006**, *9*, 444.
- [10] J. H. Nam, T. Fuse, Y. Nishi, K. C. Saraswat, *ECS Trans.* **2012**, *45*, 203.
- [11] J. A. Rogers, M. G. Lagally, R. G. Nuzzo, *Nature* **2011**, *477*, 45.
- [12] M.-J. Tsai, K.-H. Peng, C.-J. Sun, S.-C. Yan, C.-C. Hsu, Y.-R. Lin, Y.-H. Lin, Y.-C. Wu, *IEEE J. Electron Devices Soc.* **2019**, *7*, 1133.
- [13] A. Hara, Y. Nishimura, H. Ohsawa, *Jpn. J. Appl. Phys.* **2017**, *56*, 03BB01.
- [14] S. Uchikoga, *MRS Bull.* **2002**, *27*, 881.
- [15] G. Petrucci, D. Caputo, N. Lovocchio, F. Costantini, I. Legnini, I. Bozzoni, A. Nascetti, G. de Cesare, *Biosens. Bioelectron.* **2017**, *93*, 315.



- [16] A. Nathan, A. Ahnood, M. T. Cole, S. Lee, Y. Suzuki, P. Hiralal, F. Bonaccorso, T. Hasan, L. Garcia-Gancedo, A. Dyadyusha, S. Haque, P. Andrew, S. Hofmann, J. Moultrie, D. Chu, A. J. Flewitt, A. C. Ferrari, M. J. Kelly, J. Robertson, G. A. J. Amaratunga, W. I. Milne, *Proc. IEEE* **2012**, *100*, 1486.
- [17] S. Huang, Y. Liu, Y. Zhao, Z. Ren, C. F. Guo, *Adv. Funct. Mater.* **2019**, *29*, 1805924.
- [18] W. S. Wong, A. Salleo, *Flexible Electronics: Materials and Applications*, Springer, Berlin **2009**.
- [19] J. Tang, C. Y. Wang, F. Xiu, Y. Zhou, L. J. Chen, K. L. Wang, *Adv. Mater. Sci. Eng.* **2011**, *2011*, 316513.
- [20] S. Kral, C. Zeiner, M. Stöger-Pollach, E. Bertagnolli, M. I. den Hertog, M. Lopez-Haro, E. Robin, K. El Hajraoui, A. Lugstein, *Nano Lett.* **2015**, *15*, 4783.
- [21] K. El Hajraoui, M. A. Luong, E. Robin, F. Brunbauer, C. Zeiner, A. Lugstein, P. Gentile, J.-L. Rouvière, M. D. Hertog, *Nano Lett.* **2019**, *19*, 2897.
- [22] K. Usuda, Y. Kamata, Y. Kamimuta, T. Mori, M. Koike, T. Tezuka, *Appl. Phys. Express* **2014**, *7*, 056501.
- [23] T. Naito, T. Ishida, T. Onoduka, M. Nishigoori, T. Nakayama, Y. Ueno, Y. Ishimoto, A. Suzuki, W. Chung, R. Madurawe, S. Wu, S. Ikeda, H. Oyamatsu, in *2010 Symp. on VLSI Technol. IEEE, Honolulu, HI, USA* **2010**, pp. 219–220.
- [24] J. H. Parker, D. W. Feldman, M. Ashkin, *Phys. Rev.* **1967**, *155*, 712.
- [25] H. Richter, Z. P. Wang, L. Ley, *Solid State Commun.* **1981**, *39*, 625.
- [26] P. Borowicz, M. Latek, W. Rzdokiewicz, A. Łaszcz, A. Czerwinski, J. Ratajczak, *Adv. Nat. Sci. Nanosci. Nanotechnol.* **2012**, *3*, 045003.
- [27] M. De Luca, I. Zardo, in *Raman Spectroscopy and Applications*, InTech, London **2017**.
- [28] T.-H. Chang, C. Chang, Y.-H. Chu, C.-C. Lee, J.-Y. Chang, I.-C. Chen, T. T. Li, *Int. J. Photoenergy* **2014**, *2014*, 906037.
- [29] P. Rastogi, T. Dutta, S. Kumar, A. Agarwal, Y. S. Chauhan, *IEEE Trans. Electron Devices* **2015**, *62*, 3575.
- [30] D. C. Giancoli, *Physics for Scientists and Engineers with Modern Physics*, Pearson Education, London **2008**.
- [31] D. K. Ferry, S. Goodnick, J. Bird, *Transport in Nanostructures*, Cambridge University Press, Cambridge **2009**.
- [32] W. Steinhögl, G. Schindler, G. Steinlesberger, M. Engelhardt, *Phys. Rev. B* **2002**, *66*, 075414.
- [33] A. P. Graham, K. Richter, T. Jay, W. Weber, S. Knebel, U. Schröder, T. Mikolajick, *J. Appl. Phys.* **2010**, *108*, 104508.
- [34] C. Durkan, M. E. Welland, *Phys. Rev. B* **2000**, *61*, 14215.
- [35] S. M. Sze, K. N. Kwok, *Physics of Semiconductor Devices*, Wiley, New Jersey **2006**.
- [36] K. Usuda, Y. Kamata, Y. Kamimuta, T. Mori, M. Koike, T. Tezuka, in *2014 IEEE International Electron Devices Meeting*, Vol. 6, IEEE, Piscataway, NJ **2014**, pp. 16.
- [37] V. K. Khanna, in *Extreme-Temperature and Harsh-Environment Electronics: Physics, Technology and Applications*, IOP Publishing, Bristol **2017**.
- [38] D. A. Neamen, *Semiconductor Physics and Devices: Basic Principles*, McGraw-Hill, New York **2012**.
- [39] C. Wang, Y. Hu, C. M. Lieber, S. Sun, *J. Am. Chem. Soc.* **2008**, *130*, 8902.
- [40] S. Karim, K. Maaz, G. Ali, W. Ensinger, *J. Phys. D: Appl. Phys.* **2009**, *42*, 185403.
- [41] D. Aherne, A. Satti, D. Fitzmaurice, *Nanotechnology* **2007**, *18*, 125205.
- [42] J. Patterson, B. Bailey, *Solid-State Physics: Introduction to the Theory*, Springer, Berlin **2010**.
- [43] F. M. Brunbauer, E. Bertagnolli, J. Majer, A. Lugstein, *Nanotechnology* **2016**, *27*, 385704.
- [44] T. Hanrath, B. A. Korgel, *J. Phys. Chem. B* **2005**, *109*, 5518.
- [45] A. B. Greytak, L. J. Lauhon, M. S. Gudiksen, C. M. Lieber, *Appl. Phys. Lett.* **2004**, *84*, 4176.
- [46] S. Zhang, E. R. Hemesath, D. E. Perea, E. Wijaya, J. L. Lensch-Falk, L. J. Lauhon, *Nano Lett.* **2009**, *9*, 3268.
- [47] T. Imajo, K. Moto, K. Yamamoto, T. Suemasu, H. Nakashima, K. Toko, *ECS Trans.* **2020**, *98*, 423.
- [48] M. Tao, D. Udeshi, S. Agarwal, E. Maldonado, W. P. Kirk, *Solid-State Electron.* **2004**, *48*, 335.
- [49] M. Sistani, P. Staudinger, A. Lugstein, *J. Phys. Chem. C* **2020**, *124*, 19858.
- [50] H. Ko, K. Takei, R. Kapadia, S. Chuang, H. Fang, P. W. Leu, K. Ganapathi, E. Plis, H. S. Kim, S.-Y. Chen, M. Madsen, A. C. Ford, Y.-L. Chueh, S. Krishna, S. Salahuddin, A. Javey, *Nature* **2010**, *468*, 286.
- [51] K. Winkler, E. Bertagnolli, A. Lugstein, *Nano Lett.* **2015**, *15*, 1780.
- [52] L. Zhang, H. Li, Y. Guo, K. Tang, J. Woicik, J. Robertson, P. C. McIntyre, *ACS Appl. Mater. Interfaces* **2015**, *7*, 20499.
- [53] C. On Chui, K. C. Saraswat, in *Germanium-Based Technologies*, Elsevier, Amsterdam **2007**, pp. 295–361.
- [54] J. Trommer, A. Heinzig, U. Mühle, M. Löffler, A. Winzer, P. M. Jordan, J. Beister, T. Baldauf, M. Geidel, B. Adolph, E. Zschech, T. Mikolajick, W. M. Weber, *ACS Nano* **2017**, *11*, 1704.