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International Electrostatic Discharge Workshop

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Technical Sessions continued

Technical Session C: Device Physics and Testing

C.1 An ESD Protection Device with Floating P+ Diffusion for Tunable ESD Design Window and High Latch-up Immunity

Prantik Mahajan, Satya Suresh, Xiao Mei Elaine Low, Kyongjin Hwang, Robert Gauthier, GLOBAL-FOUNDRIES

Effective Supply Pin ESD protection with power clamp design incorporating Drain side Floating P+ Diffusion is presented. Conventional MV GGNMOS is typically limited in voltage applications. Tunability of the trigger and holding voltages is key to developing ESD protection power clamps with high Latch-up immunity covering a wide voltage spectrum.

C.2 Study of vfTLP Characteristics of ggNMOS in Advanced Bulk FinFET Techonology

Wen-Chieh Chen, Guido Groeseneken, KU Leuven, imec; Shih-Hung Chen, Dimitri Linten, imec

To investigate the impact of faster transient on the bulk FF GGNMOS, the vfTLP test results are shown in this work. The gate length dependence is demonstrated by vfTLP measurements and 3D TCAD simulations. Furthermore, the comparison of vfTLP and TLP results are presented.

C.3 Impact of Extreme Wafer Thinning on Latch-up (LU) Risk in Advanced CMOS Technologies

Kateryna Serbulova, Guido Groeseneken, KU Leuven, imec; Shih-Hung Chen, Dimitri Linten, imec

Latchup (LU) risk in advanced technologies cannot be eliminated and even becomes one of the major reliability concerns, especially for stacking architectures with extremely thinned Si substrate. LU originates from parasitic BJTs forming SCR path. In this work the current gain is evaluated for two parameter variations in TCAD simulations.

C.4 Influencing SCR Holding Current by Segmentation Topology

Vasantha Kumar, Steffen Holland, Hans-Martin Ritter, Nexperia; Hasan Karaca, Dionyz Pogany, TU Wien

A segmented layout topology on a novel SCR is used to obtain a higher holding current (Ihold). The SCR Ihold has been increased by reducing the emitter area of the PNP, which reduces the injection efficiency of the PNP. The increased ability to collect free carries results in higher Ihold.

C.5 Efficient 3.3V Power Clamp Circuit Using Low-Voltage 1.2V Transistors in CMOS Process

Ranabir Dey, Vijaya Kumar Vinukonda, Fabrice Blanc, Arm

Some 5nm technology goes with 1.2V thick-oxide devices. So triple-stack ESD clamps are needed to support 3.3V operation. As traditional stacked-clamp ESD efficiency is not optimum, a new 3.3V stacked-clamp with multi-gates RC trigger circuit is proposed. Better ESD clamping voltage efficiency is shown while keeping almost the same area footprint.

C.6 Co-Optimization on RF/High-Speed I/O Pad: Efficient ESD Solution for 5G Heterogeneous Stacking Interface in Advanced CMOS Technology

Wei-Min Wu, KU Leuven, NCTU, imec; Shih-Hung Chen, Marko Simicic, Dimitri Linten, imec; Ming-Dou Ker, NCTU; Guido Groeseneken, KU Leuven, imec

In the 5G broadband ESD design, moving first-stage ESD devices under I/O pads resulted in better ESD performance. However, extra parasitic capacitance was increased to RF bandwidth degradation. Therefore, ESD diodes layout optimization was proposed to enable capacitance and HBM improvement. CDM evaluation is also discussed for wafer-to-wafer integration issue

C.7 Triggering of Multi-Finger and Multi-Segment SCRs Near the Holding Voltage Studied by Emission Microscopy Under DC Conditions

Hasan Karaca, Rudolf Krainer, Dionyz Pogany, TU Wien; Clement Fleury, Silicon Austria Labs; Steffen Holland, Hans-Martin Ritter, Vasantha Kumar, Guido Notermans, Nexperia

Emission microscopy under DC current controlled mode has been used to study current flow distribution in multi-finger and multi-segment SCRs. The elements trigger at nearly the same current density indicating the substrate-coupled triggering mechanism found previously under TLP regime. On-resistance and holding current aspects are also discussed.