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A Top-Down Platform Enabling Ge Based Reconfigurable Transistors

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Conventional field-effect transistor (FET) concepts are limited to static electrical functions and demand extraordinarily steep and reproducible doping concentration gradients. Reaching the physical limits of scaling, doping-free reconfigurable field-effect transistors (RFETs) capable of dynamically altering the device operation between p- or n-type, even during runtime, are emerging device concepts. In this respect, Ge has been identified as a promising channel material to enable reduction of power consumption and switching delay of RFETs. Nevertheless, its use has been limited to simulations and bottom-up demonstrators not compatible with complex circuit technology. In this work, a deterministic top-down fabrication scheme is demonstrated to realize a Ge-based RFET architecture and exploring realizations with three independent gates. Polarity control and leakage current suppression are enabled by the specific injection of charge carriers through gated Al-Ge heterojunctions and the introduction of a blocking electrostatic energy barrier. Further, the choice of monolithic Al/Ge contacts alleviates process variability compared to Ni-germanide contacts presenting a top-down technology platform for Ge-based RFETs. Our device concept is a first step toward future integrated high-performance and low-power reconfigurable circuits, providing a platform for future energy-efficient systems as well as hardware security integrated circuits.

1. Introduction

In conventional integrated circuit (IC) devices, logic functions are fixed by the physical layout and the definition of doped regions and thus do not allow a reconfiguration of the circuit. A popular approach to overcome this limitation is the course-grain reconfiguration, i.e. the signal routing to predefined logic blocks as practiced in field programmable gate arrays (FPGA).[1] This approach nevertheless leads to a high latency in data transfer and substantial chip area consumption since few active regions are not utilized at once. Distinctly, the *ansatz* of reconfiguration of elementary function blocks, i.e. the *fine-grain* reconfiguration, gives rise to a paradigm change where devices and circuits are actively redesigned after manufacturing and noteworthy even at runtime. Thereto, combinational circuits have shown benefits in area and power consumption by reconfiguration of complete logic blocks.[2]

The building blocks for such circuits are RFETs, capable of merging the electrical properties of unipolar p- and n-type FETs into a single type of device with identical technology, geometry and composition.[3–5] Notably, RFETs do not require doping in contrast to classical FETs. Thereto, a device layout with independent gates is used to induce an additional energy barrier to the channel that blocks the undesired charge carrier type and therefore favors p- or n-type operation respectively. Consequently, reducing the technological fabrication complexity, they enable dynamic programming of circuits at the device level.[3,5] Prominent applications of such RFET devices are currently arising in the area of hardware security[6] and in highly integrated combinational and sequential logic.[5,7]

Different channel materials have been employed to realize RFETs. With the use of Si channels and Ni_xSi_{1-x} contacts various concepts with two or more independent gates have been proven experimentally.[8–11] Remarkably, symmetry in the output characteristics of p- and n-operation has been reached by the use of strain engineering both on bottom-up[12] and top-down Si nanowire RFETs[13]. Despite those outstanding efforts it has been noted, that the enhancement of the drive current and the reduction of dynamic power consumption strongly scales with the reduction of the respective Schottky barrier heights for electrons and holes. In this sense, Ge and SiGe have been identified as promising channel materials due to their reduced bandgap compared to the one of Si. Since the highest fraction of transport relevant for device and circuit performance is dictated by quantum mechanical tunneling of charge carriers[12] the use of Ge and Si_xGe_{1-x} channels

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of high Ge content is expected to enhance the injection of both electrons and holes and thus holds the promise to translate into higher on-currents and faster switching.[14] Further details on the tunneling mechanism and choice of Ge semiconductors are highlighted in the supporting information. Indeed, recent mixed-mode device TCAD calculations highlight the potential of Ge versus Si RFETs in terms of ring oscillator frequency, a figure of merit. Its value at equal power consumption can be scaled up substantially.[15] First Ge nanowire RFETs with reduced threshold voltages have been readily shown.[16] Nevertheless, this technology is based on bottom-up nanowires where deterministic positioning, control of crystal orientation, patterning and nanowire size control is challenging. Moreover, these devices suffer from an inherent variability in phase formation of the used nanometer scale Ni-germanide contacts[16–19] leading to different barrier heights and electrical characteristics. Thereto, a top-down Ge RFET technology platform necessary to deliver low variability and deterministic capability to fabricate demonstrator circuits has been pending.

In this paper, a deterministic top-down Ge RFET technology capable of suppressing the high leakage current in Ge nanodevices is proposed employing a Ge on insulator (GeOI) integration scheme that can be principally scaled up to wafer size. Also differently than in prior RFET art based on Ni-germanide contacts[16] monolithically integrated Al-Ge-Al heterostructures are employed. Its use overcomes the difficulty in reproducibly and deterministically defining the metallic phase[17] of the source and drain junctions solving the aforementioned phase stability issues of conventional Ni-germanide contacts. Moreover, in contrast to common-metal-germanide/-silicide alloy formation, the Al-Ge exchange results in a highly conducting and pure metal with abrupt semiconductor/metal heterostructure contacts.[20,21]

2. Results and Discussion

We present a top-down approach to fabricate monolithic Al-Ge-Al heterostructures with abrupt metal-semiconductor junctions embedded in an RFET device architecture. Without limiting the generality for parallel processing, **Figure 1**a shows exemplarily the fabrication scheme for an individual Al-Ge-Al heterostructure device. First, the 75 nm thick device layer of a ⟨100⟩-oriented GeOI substrate is patterned into a mesa structure using common electron beam lithography (EBL) and reactive ion etching (RIE). A scanning electron microscopy (SEM) image of an etched Ge nanosheet is shown in Figure 1b. Using atomic layer deposition (ALD), the Ge nanosheets are capped by a 22 nm thick Al_2O_3 passivation layer. Al contact pads are fabricated by optical lithography, Al_2O_3 and native oxide removal, sputter deposition and lift-off techniques (see Experimental Section). Finally, the actual heterostructure formation is induced by well controlled rapid thermal annealing (RTA) in forming gas atmosphere, resulting in the encroachment of the Al leads within the Ge layer by an exchange reaction, thereby contacting the remaining Ge channel.[20,22] A respective SEM image of the complete Al-Ge-Al nanowire-like heterostructure is shown in Figure 1c. Cross-sectional (scanning) transmission electron microscopy ((S)TEM) images of the right-side Ge-Al heterojunction are shown in Figure 1d,e. Both the STEM and HRTEM images reveal a sharp interface with finite (atomic level) roughness at the Al-Ge junction that is inclined with respect to the viewing direction and does not show any indications of chemical intermixing. Based on extensive TEM investigations on the Al-Ge exchange for vapor-liquid-solid grown Ge nanowires and top-down fabricated Ge nanosheets,[21] it was shown that the Al propagation is governed by Ge diffusion via surface channels on the Al to the extended contact pads. The Al replacing the Ge is thereby provided by effective Al self-diffusion. This mechanism is based on the asymmetric diffusion coefficients of the material system. While the diffusion of Ge in Al as well as self-diffusion (Al in Al) is rather fast, the diffusion of Al in Ge is extremely slow (see Table S1, Supporting Information). Thus Al contamination in Ge is unlikely.[21] Figure 1d,e shows representative TEM images of a monolithic Al-Ge-Al heterostructure, with the interface being composed of a Ge {111} and an

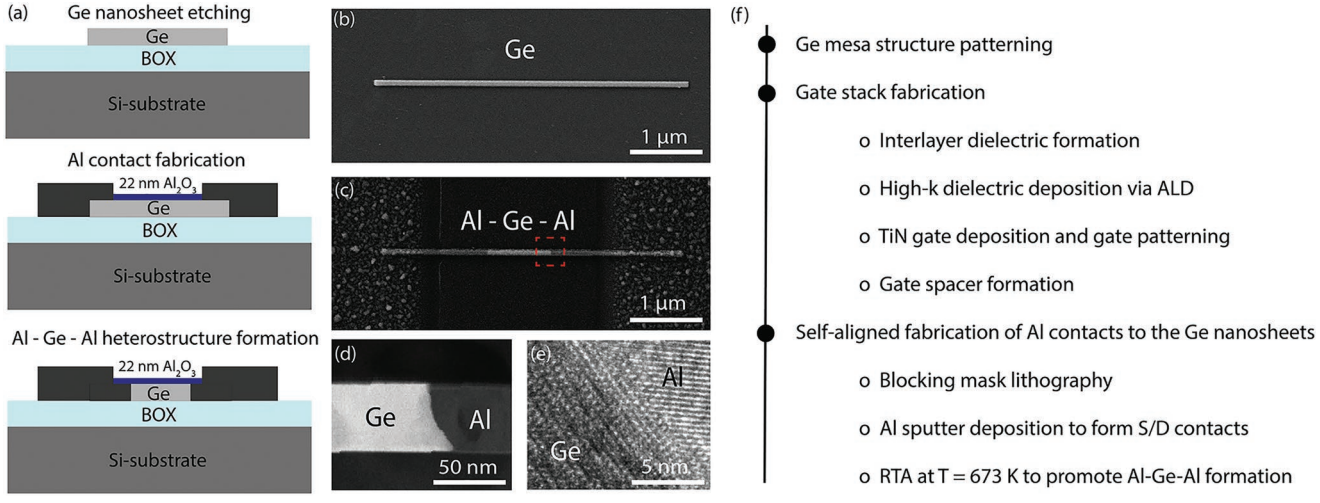

Figure 1. a) Processing scheme for the wafer-scale fabrication of Al-Ge-Al heterostructures. b) SEM image of the etched and isolated Ge nanosheet mesa structure. c) SEM image of the Al-Ge-Al heterostructure after RTA. d) Cross-sectional STEM image of the Ge-Al interface indicated by the red dashed box in (c). e) HRTEM image showing the abrupt Ge-Al heterojunction. f) Proposed wafer-scale fabrication scheme of Al-Ge-Al heterostructure nanosheet devices.

Al {200} facet, respectively. While both crystals are oriented in a [110] zone axis, a mutual in-plane rotation of 6.5° was measured, which might be associated to strain compensation and lattice relaxation to accommodate the lattice mismatch between Ge and Al.[21]

To underline the composition of the device stack, an EDX map of the fabricated device is shown in Figure S1 (Supporting Information). Further details regarding the evidence and characterization of Al-Ge-Al heterostructures, i.e. energy dispersive X-ray spectroscopy (EDX) and electron backscatter diffraction (EBSD) investigations can be found in the work of Wind and Sistani et al.[21]

An example for a prospective wafer-scale fabrication process of Al-Ge-Al heterostructure nanosheet transistors is shown in Figure 1f. Thereto, the mesa structure is patterned using lithography and RIE. Further, a high-k dielectric is deposited by ALD. The gate stack is finalized by TiN deposition and gate patterning. The self-aligned Al contacts are fabricated by using blocking mask lithography and Al sputter deposition, followed by RTA to promote the Al-Ge-Al formation.

Next, we focus on the electrical properties of the Al-Ge-Al nanosheets. Assuming thermionic emission, the effective Schottky barrier height of the Al-Ge junction using the p-doped Si handle wafer as back-gate was estimated from the slope of the activation energy plot of $\ln(J/T^2)$ versus $1000/T$ (Arrhenius plot) at various bias and back-gate voltages. The thereof calculated effective barrier height is shown in Figure S2 (Supporting Information), revealing a strong asymmetry regarding the barrier for electrons and holes of the Al-Ge heterojunction, indicating strong Fermi level alignment close to the valence band.[23,24]

Adding an omega-shaped top-gate atop the intrinsic Ge channel, **Figure 2** shows the Al-Ge-Al heterostructure integrated into a FET architecture, for clarity we name this device the single top-gated transistor. Figure 2a,b shows a schematic and a colored SEM image of such a single top-gated device with a Ge channel length of L_{Ge} = 1.90 µm and a structural width of W = 270 nm. Note that for the top-gate dielectric Al_2O_3 with a thickness of 22 nm was used. As the top-gate covers the whole channel (incl. Al-Ge junctions) no back-gate potential is necessary. Figure 2c shows a schematic representation of the band structure of the single top-gated heterostructure device. For negative gate-voltages, the combination of Fermi level alignment close to the valence band and upward band banding results in a strongly hole-dominated transport. In contrast, positive gate voltages, result in downward band banding and electron-dominated transport.[25]

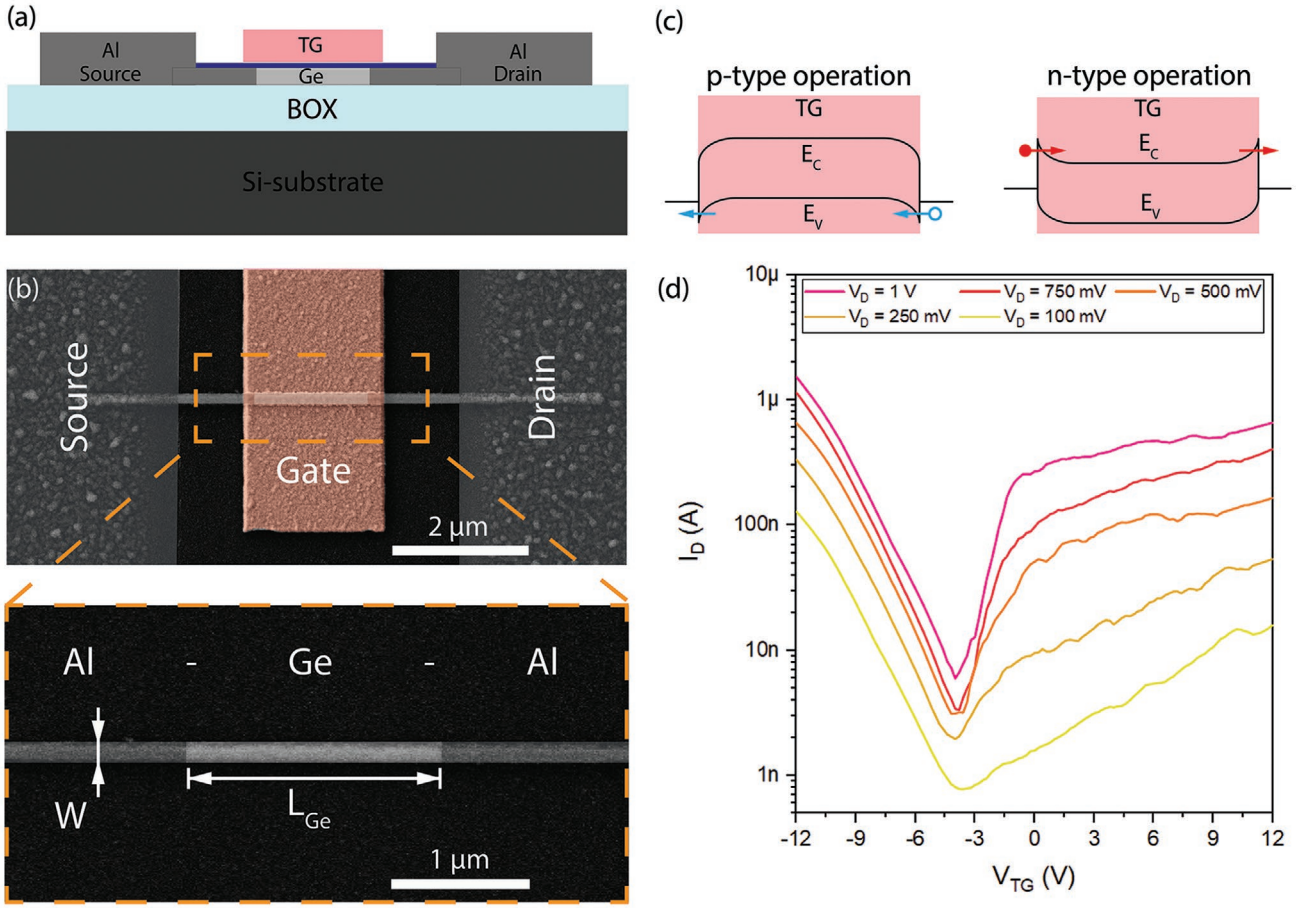

Figure 2. a) Schematic of an Al-Ge-Al heterostructure embedded in an omega-shaped single top-gate FET architecture. b) Colored SEM image of a single top-gated device with L_{Ge} = 1.90 µm and W = 270 nm. The top-gate dielectric consists of 22 nm Al_2O_3. c) Band diagrams of p- and n-type operation. d) Transfer characteristic of a single top-gated device for bias voltages between V_D = 100 mV and 1 V.

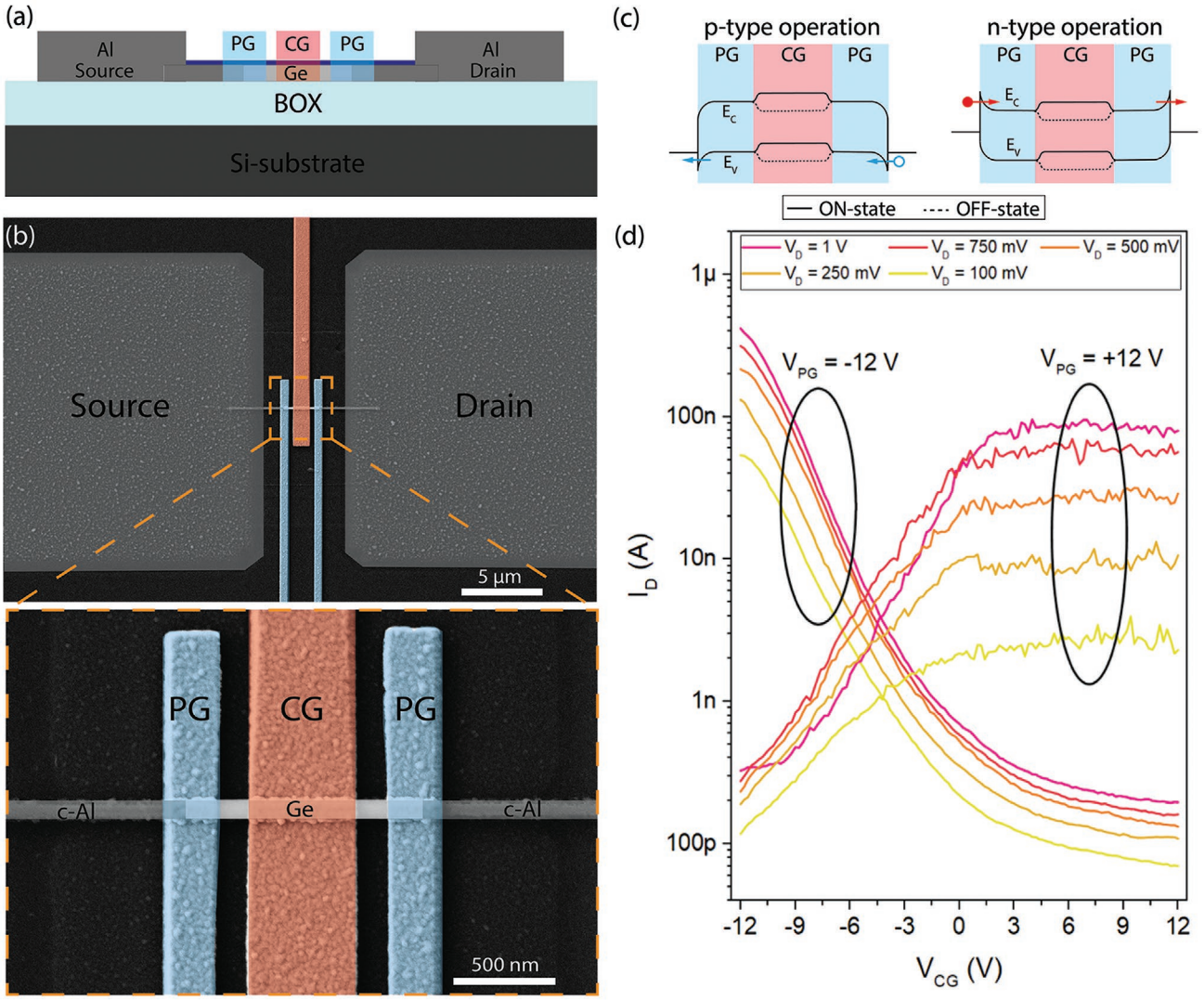

Figure 3. a) Schematic of an Al-Ge-Al heterostructure with $L_{Ge} = 2.10$ µm and $W = 180$ nm embedded in a three-independent top-gated FET architecture enabling RFET operation. The top-gate dielectric consists of 22 nm Al_2O_3. b) Colored SEM image of a three-independent top-gated device. c) Schematic band diagrams showing p- and n-type device operation. d) Transfer characteristic of a representative RFET device for different bias voltages between $V_D = 100$ mV and 1 V showing unipolar p- and n-type operation as programmed by V_{PG}.

Consequently, as exemplarily shown in Figure 2d, biasing the single top-gated Al-Ge-Al heterostructure device exhibits an ambipolar transfer characteristic, which was obtained for bias voltages between $V_D = 100$ mV and 1 V indicating an I_{ON}/I_{OFF} ratio of approximately 10^2. This behavior is expected and is an elemental device ingredient to reach polarity control when steered with additional gates as detailed below. Further, detailed transport maps $\log(|I_D|(V_{TG}, V_D))$ in Figure S5, Supporting Information) underline the ambipolar behavior of the single top-gated device architecture. At $V_D = 1$ V peak current densities of $J_h = 10327$ A cm^{-2} (holes) and $J_e = 4428$ A cm^{-2} (electrons) were calculated. The off-current at $V_{TG} = -3.8$ V results in a current density of $J_{OFF} = 39.55$ A cm^{-2}.

To embed the Al-Ge-Al heterostructure in an RFET architecture, three independent omega-shaped top-gates were added to the device as shown in **Figure 3**a: Two aligned on top of the two Al-Ge heterojunctions and one in the middle of the Ge channel. Previous works[9,12] have shown that the capability of a two top-gate RFET merely changes the shape, i.e. the thickness of the injection barrier at source and thus translates into a degraded inverse subthreshold slope versus the one of a conventional FET. Under the prerequisite of utilizing an ultrathin high-k gate dielectric and fully optimized device geometry, an additional gate in the middle of the Ge channel, the energy barrier is moving linearly with the gate voltage of the middle top-gate enabling an improved subthreshold slope in the same regime as of a conventional FET (65 mV dec^{-1} at 300 K). A comparison of the two approaches is shown in Figures S3 (two top-gates, Supporting Information) and S4 (three top-gates, Supporting Information).

Depending on the voltage applied to the gates, atop the abrupt Al-Ge heterojunctions, either hole or electron transport can be set. This leads to the pursued polarity control, which allows to select p- or n-type operation of the RFET. In this respect, these gates are further denoted program-gates (PG), as the dedicated mode can be programmed in a volatile manner.

Further, the gate aligned in the middle of the Ge channel serves as a control-gate (CG), turning the transistor conductance on or off.

In p-type configuration, the device is programmed by setting V_{PG} = –12 V. Transfer measurements ($I_D(V_{CG})$) were performed by sweeping V_{CG} from –12 to 12 V for fixed bias voltages between V_D = 100 mV and 1 V (see p-type operation in Figure 3d). Accordingly, the negative potential on the PG effectively blocks electron injection from the drain electrode. Further, it enables unipolar p-type operation as the upward band bending below the PG stimulates hole injection into the active region. By sweeping V_{CG}, it is thus possible to turn the transistor on (negative V_{CG}) and off (positive V_{CG}) by regulating the thermionic emission of the injected charge carriers though the channel region as in a conventional FET. To switch to n-type operation, V_{PG} = 12 V is applied, which favors electron injection. Its functionality was verified again by a V_{CG} sweep from –12 to 12 V for fixed bias voltages between V_D = 100 mV and 1 V (see n-type operation in Figure 3d). In this configuration, the voltage V_{PG} sets the junction transparent for electrons and effectively blocks the injection of holes into the Ge channel. Consequently, sweeping V_{CG}, the transistor can be turned on (positive V_{CG}), or off (negative V_{CG}), enabling unipolar n-type FET operation. Note that the on-current of the n-type program shows a high variation over different applied drain voltages V_D, which is typical for Schottky FETs, given the supra-linear output characteristic for low V_D.[26] The disparity in the output characteristic behavior between p- and n-type is associated to the asymmetric Schottky barrier heights (see Figure S6, Supporting Information). This behavior also correlates perfectly with the shown data in Figure S2 (Supporting Information) as a respective energy barrier is visible for n-type operation, whereas in the p-type operation no barrier is visible. We want to note that for the future implementation of the presented RFETs into logic circuits, a reduction of the supply voltages for the polarity and control gates can be achieved by the use of thinner high-k interface dielectrics (here: 22 nm Al_2O_3), ideally using the same supply voltages as between source and drain.

The RFET concept shown in Figure 3 clearly shows the ability to suppress source to drain leakage currents for both program types by electrostatically tuning the band structure shape along the channel length. Compared to the single top-gate Schottky FET in Figure 2, the lowest leakage currents drop by over one order of magnitude strongly suppressing static power consumption despite the low bandgap material employed.

Applying $|V_{PG}|$ = 12 V, a total on/off-ratio of 2×10^3 and 2×10^2 is achieved for p- and n-type respectively. Further, the peak transconductance $g_m = dI_D/dV_{CG}$ is obtained, with 71 and 2 nS for p- and n-type respectively. Again, we want to note that an enhancement of the on/off-ratio is expected by the future use of thinner high-k dielectrics, decreased width and shorter Ge channel lengths. Enhancement of these values is expected by the future use of thinner high-k dielectrics and shorter channel lengths. Figure S7 (Supporting Information) shows the evaluation and extraction of the transconductance g_m. Compared to the single top-gated device architecture, the off-current densities in the RFET configuration are decreased by a factor of 20 for p- and 12 for n-operation, showing the effectiveness in introducing a blocking energy barrier to suppress source-drain leakage. In turn, the on-current densities obviously do not show any remarkable change, as the geometry of the Al-Ge-Al heterostructure certainly remained the same. Applying, V_D = 1 V, it was possible to achieve J_h = 4284 A cm^{-2} (J_h^{OFF} = 2.01 A cm^{-2}) in p-operation and J_e = 927.40 A cm^{-2} (J_e^{OFF} = 3.36 A cm^{-2}) in n-operation.

To further confirm the unipolar p- and n-type operation of our Al-Ge-Al heterostructure based RFET device, we analyzed the output characteristic (see Figure S6, Supporting Information) for both operation modes.

To elucidate the operation spaces of our RFETs. **Figure 4**a,b shows a color map of the recorded log|I_D| in dependence of V_D and V_{CG}. The region of unipolar p- and n-type on-regimes is indicated by the red dashed area. Further, the temperature dependent p- and n-type operation was investigated (see Figure 4c,d). As expected from theory, the transfer curves in the subthreshold region are flattening with increased temperature for both operation types.[27,28] Further, an increase in the off-current with temperature is evident, which can be attributed to a higher amount of thermally generated carriers that surpass the blocking barrier. Nevertheless, ambipolar operation is still well suppressed for both operation modes even at T = 360 K.

The fact that the transfer and output characteristic can either resemble a p- or a n-type FET, implies that static p- and n-type FETs in a circuit can be replaced by RFETs, principally enabling deliberate logic functions in a complementary design.[3] However, there are still problems to overcome in the presented Al-Ge material system, such as fixed charges in the Al_2O_3 gate dielectric that promote p-type conduction and the asymmetry of the Schottky barriers contribute to a difference, which contribute to a difference between the currents in p- and n-type operation. The latter is mainly attributed to the GeO_x layer between the Al_2O_3 and Ge channel, where interface traps induce a charge trapping and de-trapping dynamic, which induces a hysteresis in the I/V characteristic and degrade the mobility of the channel.[29,30] A method to overcome these issues could be for instance the removal/desorption of native GeO_x and the subsequent ordered stoichiometric thermal growth of GeO_2 and/or posterior Ge oxy-nitride formation in order to reduce the level of interface states at the dielectric/Ge interface.[31] Further, the gate and Schottky contact metal work functions and the oxide-induced compressive stress to the Schottky junction could be adjusted to lift the asymmetry of the injection barriers for holes and electrons.[13] Importantly, the possibility of changing the configuration of each transistor within a circuit enables a reconfiguration of its specific logic functions during operation.[32] Further, the bidirectional nature of reconfigurable transistors is a clear advantage for flexible and adaptive circuit design, as equivalent results can be obtained by swapping the signals between source/drain and V_{PG}/V_{CG}.[9] Considering that, simulations of multi-gate Ge-based RFET devices suggest a possible RFET operation down to a channel length of approximately L_{Ge} = 50 nm,[16] our prototyping platform may paves the way for the development of key components of high-performance and low-power reconfigurable circuits, providing a prototyping platform for future energy-efficient systems as well as hardware security integrated circuits.

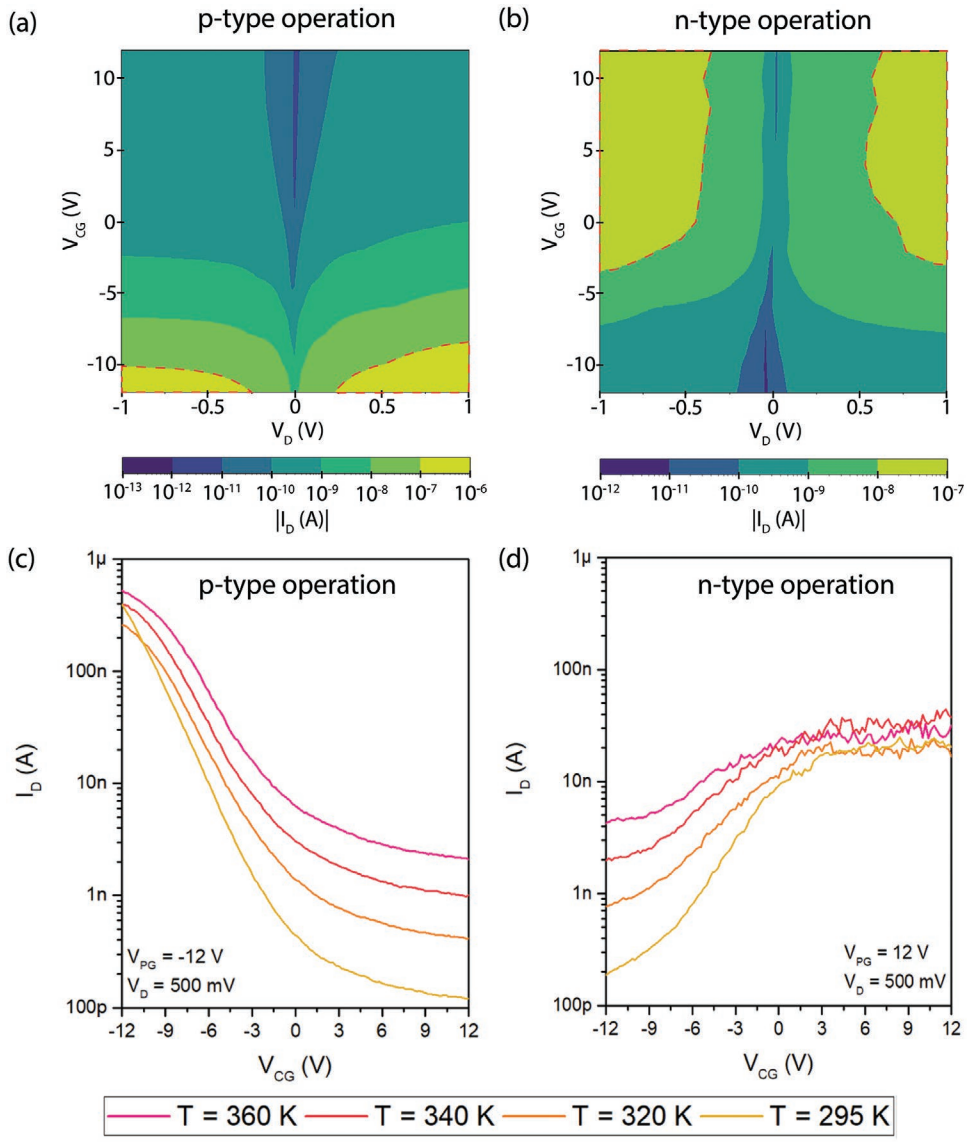

Figure 4. Drain current map versus V_{CG} and V_D ($\log|I_D|(V_{CG},V_D)$) of the Ge-based RFET device in a) p- and b) n-type operation. Stable on-operation regimes are highlighted by red dashed areas. Temperature dependent c) p- and d) n-type subthreshold transfer characteristics of the Ge-based RFET device. An increase in the off-current level and degradation of subthreshold swing with increasing temperature is visible. However, no substantial increase of the on-current was observed.

3. Conclusion

In conclusion, we have demonstrated a three-independent gate RFET based on a monolithic Al-Ge-Al heterostructure embedded in a GeOI platform. Unipolar p- and n-type operation is achieved by actively tuning the barrier transmissibility by program-gates atop sharp Al-Ge heterojunctions. A dedicated control-gate controls the charge carrier concentration in the Ge channel and thus allows to turn the transistor on and off.

By comparison with a common single top-gated FET architecture, we demonstrate that the proposed device architecture is capable of significantly reducing the off-current. At $V_D = 1$ V, we calculated peak current densities $J_h^{ON} = 4284$ A cm^{-2}/J_h^{OFF} = 2.01 A cm^{-2} and $J_e^{ON} = 927.4$ A cm^{-2}/$J_e^{OFF} = 3.36$ A cm^{-2} for the RFET device. Applying $|V_{PG}| = 12$ V, a total on/off-ratio of 2×10^3 and 2×10^2 is achieved for p- and n-type respectively. Furthermore, conducting measurements at elevated temperatures, we show that ambipolar operation is still well suppressed for both operation modes even at $T = 360$ K.

Paving the way for flexible and adaptive circuit designs based on an RFET architecture, the proposed platform provides a first step towards a beyond-CMOS approach enabling functional diversification and alternative computing approaches.

4. Experimental Section

High-resolution HAADF STEM: Samples for HR(S)TEM measurements are prepared using focused ion beam lift-out technique

in a FEI Helios Nanolab 660. HRTEM images have been acquired at an aberration corrected FEI Titan^3 80–300 microscope at 300 kV. STEM measurements have been performed at a JEOL F200 microscope operated at 200 kV.

Device Fabrication: The devices were fabricated from GeOI substrates comprising a 75 nm thick (100) oriented Ge device layer atop of a 150 nm buried SiO_2 layer and a 500 µm thick doped Si substrate. The Ge structures were patterned using EBL and a SF_6-O_2 based RIE. Subsequently, the Ge structures were coated with 22 nm of Al_2O_3 deposited by ALD. Al pads contacting the Ge nanostructures were fabricated by optical lithography, 125 nm Al sputter deposition, preceded by a 25 s BHF (7:1), 5 s HI dip (14%) to remove the Al_2O_3 and the Ge oxide, and lift-off techniques. The Al-Ge exchange reaction was induced by rapid thermal annealing at a temperature of $T = 674$ K in forming gas atmosphere. To achieve Ge devices with short segment lengths, consecutive thermal annealing steps were applied. Further, omega-shaped Ti/Au top-gates were fabricated atop Al-Ge-Al heterostructures, using a combination of electron beam lithography, Ti/Au evaporation (7 nm Ti, 125 nm Au), and lift-off techniques.

Electrical Characterization: The electrical measurements were carried out at room temperature ($T = 295$ K) and ambient conditions using a combination of a semiconductor analyzer (HP 4156B) and a probe station placed in a dark box. Source-measure units (SMU) were used for all device terminals. The gate current characteristic of the single- and three-independent-gated device is shown in Figures S8 and S9 (Supporting Information) respectively in the supporting information. Temperature dependent measurements (295–360 K) were performed in a cryogenic probe station (LakeShore PS-100) and a semiconductor analyzer (Keysight B1500A).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

R.B. and M.S. contributed equally to this work. M.S. and R.B. performed the device fabrication. R.B., M.S., and B.L. conducted the measurements. D.P. and B.R. carried out the TEM characterization and analysis. A.L. provided helpful feedback and commented on the manuscript. W.M.W conceived the project and contributed essentially to the experimental design. All authors analyzed the results and helped shape the research and manuscript.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

electrostatic doping, germanium, metal-semiconductor heterostructures, polarity control, reconfigurable transistors

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