Towards Explaining the Fault Sensitivity of Different QDI Pipeline Styles

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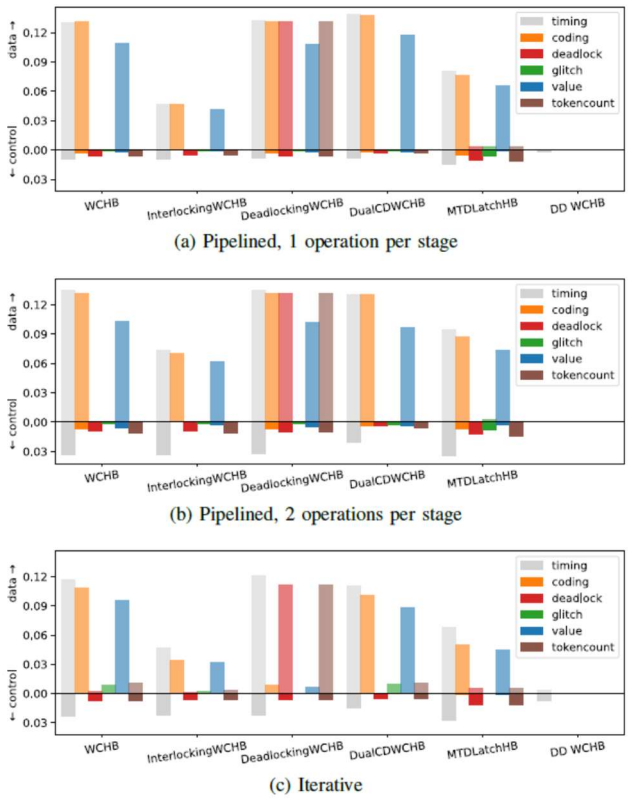
Asynchronous circuits, specifically those using a quasi delay-insensitive (QDI) implementation are known for their high resilience against timing uncertainties. However, their event based operation principle impedes their temporal masking capability, making them more susceptible to fault-induced transitions caused by single event transients. While synchronous circuits obtain high resilience through temporal masking that is established through the sampling of data by flip flops, asynchronous circuits, by design must be flexible about the phases of data validity leaving a larger attack surface for faults. Consequently, previous work has proposed to narrow down the windows in which data changes are accepted, in order to improve the temporal masking in QDI designs. Unfortunately, it is hard to combine the existing insights and results into a global picture, as they all have been derived for specific circuits and pipeline types, under specific experimental conditions (or by theoretical analyses) and with specific targets in mind.

Our vision is to elaborate such a global picture through a large experimental study (complemented by theory) that allows an apples-to-apples comparison of different pipeline styles and fault-tolerance enhancements. Since the masking effects in asynchronous design seem to depend on many operational parameters like the pipeline fill level, or the data being processed, another target is the identification of such factors along with a modeling of their specific influence. On the foundation of this understanding, we can then identify the main vulnerabilities, the most efficient existing enhancement approaches, and finally elaborate further improvements. In this paper we report about some first important steps in this direction. We present an experimental environment that allows the convenient generation of target circuit descriptions, as well as the fully automated conduction of large gate-level simulation experiments with millions of fault injections, while still providing the ability to precisely reproduce each single fault injection for closer inspection of interesting cases. Using this tool we perform a detailed comparison of fault effects seen in different QDI pipeline styles (variants of the weak condition half buffer (WCHB) and Mousetrap-style D-latch half buffer), for a multiplier with varying bit width implemented in delay-insensitive minterm synthesis (DIMS) with randomized delays. Beyond different levels of pipelining we also consider an iterative circuit topology, and we vary the pipeline fill level in several steps from token limited to bubble limited.



(a) Pipelined, 1 operation per stage

(b) Pipelined, 2 operations per stage

(c) Iterative

Figure-1: Number of observed effects relative to the total number of injections for 8 bit multiplier designs

Figure 1 shows an example of our results, where, e.g. good robustness of the interlocking WCHB can be observed, low sensitivity of control signals relative to data signals, as well as interesting differences between linear pipeline and iterative implementation. More generally, our results allow to study the relative sensitivity of circuits resulting from different design choices.