We are pleased to announce the Nanowire Week 2022. The 4th workshop of this series which resulted from the merge of two well-established and highly successful annual workshops:

NANOWIRES and Nanowire Growth Workshop

-Starting in Lund, Sweden (2017), the Nanowire Week symposium has since been held in Hamilton, Ontario, Canada (2018) and in Pisa, Italy (2019).

The Nanowire Week 2022 will be held at the Congress Center in Chamonix, France, in April 2022 from the 25th to the 29th.

Chamonix is a beautiful mountain resort in the French Alps, located at an altitude of 1035 m, at the foot of Mont Blanc. It is only 1 hour away from Geneva airport, less than 2 hours from Lyon airport, and the 11.6 km Tunnel du Mont-Blanc offers rapid road access to Italy’s Aosta Valley.

Nanowire Week is a unique venue for discussions regarding progress of nanowire-related research from growth and fundamental studies to applications.

Main topics include:

- Nanowire synthesis
- Nanowire growth modeling
- Heterostructures and alloys
- Arrays, networks and hierarchical systems
- Advanced microscopies and spectroscopies applied to nanowires
- Optical, electrical, thermal and mechanical properties
- Electron transport and doping in nanowires
- Quantum behaviors and devices
- Nanowire integration into functional materials
- Hybrid nanowire-biological systems
- Sensors and actuators
- Electronic and optoelectronic devices
- Energy conversion and storage

Conference Proceedings:

11h45 – 12h00  Michael Seifner, 
*Biaxial Nanowire Heterostructure Growth facilitated by two-phase Seed Particles*,
Lund University, Sweden.  p.61

12h00 – 12h35  Exhibitors

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12h40 – 14h00  Lunch break

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**Tuesday, April 26, Afternoon**

**14h00-16h00  Poster session 1**

**Session 7 Devices  Chair: Francesco ROSSELLA**

**16h00 – 16h30**  Andrea Cattoni,
*Selective-area growth of III-V nanowire arrays on silicon and their application for tandem solar cells*,
C2N-CNRS & IPVF, Palaiseau, France.
Invited  p.63

**16h30 – 16h45**  Masiar Sistani,
*Programmable negative differential Resistance in Ge Nanowire Transistors*,
Institute of Solid State Electronics, TU Wien, Vienna, Austria.p.64

**16h45 – 17h00**  Simone Assali,
*GeSn Nanowire Mid-Infrared Optoelectronic Devices*,
Engineering Physics, Montreal, Canada.  p.65

**17h00 – 17h15**  Dags Olsteins,
*On-chip multiplexing enabled by SAG nanowire transistors*,
University of Copenhagen, Denmark.  p.66
## Session 7 Devices  
**Chair: Francesco ROSSELLA**

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Programmable negative differential Resistance in Ge Nanowire Transistors

Masiar Sistani\(^1\), Raphael Böckle\(^3\), Minh Anh Luong\(^2\),
Martien I. den Hertog\(^3\), Alois Lugstein\(^3\) and Walter M. Weber\(^3\)

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Contact: masiar.sistani@tuwien.ac.at

The functional diversification and adaptability of the elementary switching units of computational circuits are disruptive approaches for advancing electronics beyond the static capabilities of conventional CMOS. In this respect, two emerging concepts in electronics are doping-free reconfigurable FETs (RFETs) capable of dynamically altering the device operation between p- and n-type and multi-valued logic (MVL), replacing conventional binary systems by operation schemes with radices or bases higher than two. Thereo, a highly interesting transport mechanism is the transferred electron effect, enabling negative differential resistance (NDR) by the scattering of electrons from the energetically favorable low effective mass conduction band valley to a heavy mass valley nearby. Here, we exploit the nanometer scale properties of Ge nanowires (NWs) with unique monocrystalline Al contacts to deliver a strong and reproducible NDR effect at room temperature. Notably, we found a factor 10 larger peak-to-valley ratio compared to state of the art Si/SiGe resonant tunneling diodes and a stable NDR operation up to \( T = 360 \) K, which is an important prerequisite for realistic logic applications [1]. Embedded into a three-gate FET architecture, the one-dimensional nature of monocrystalline and monolithic Al-Ge based NW heterostructures is exploited to not only deliver charge carrier polarity control but furthermore to enable distinct programmable NDR at runtime [2]. This so called NDR-mode RFET provides a unique fusion of the concept of reconfiguration and NDR embedded in a universal adaptive transistor that may enable energy efficient programmable circuits with multi-valued operability that are inherent components of artificial intelligence electronics.

![Figure 1 (left)](image1.png) Colored SEM image of a three-gate Ge FET. The insets show HRTEM images of the Al-Ge-Al NW heterostructure. (right) I/V output characteristic of the device showing the ability to shift NDR region with respect to the gate-voltage. The inset depicts a schematic representation of the band structure of Ge with indicated electron transfer from the L-valley into the X-valley enabling NDR.
