Method to Distinguish Between Buffer and Surface Trapping in Stressed Normally-ON GaN GITs Using the Gate-Voltage Dependence of Recovery Time Constants

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***Abstract*— Drain current recovery transients are analyzed in normally-ON (NON) gate injection transistors (GITs) subjected to different kinds of stress. The recovery is measured as a function of forward gate bias, V_G, which controls the number of holes injected from the gate and speeds up the recovery. Unlike conventional normally-OFF GITs, the newly designed NON GIT test structures allow simple characterization of buffer trapping during back-gating. By comparing the V_G-dependence of recovery time constants for OFF-state and semi-ON state stress with those obtained from back-gating experiments we are able to distinguish between buffer and surface trapping. Our approach is simple and does not require time-consuming temperature-dependent measurements. It is found that OFF-state stress causes negative charge accumulation in the buffer, while semi-ON state stress leads to accumulation in both, buffer and surface. The use of NON GITs enables to measure the recovery time constants related to the buffer over a wide span of six orders of magnitude (10^{-4}–100 s).**

***Index Terms*— Buffer trapping, dynamic ON-resistance, gallium nitride (GaN), gate injection transistor (GIT), high electron mobility transistor, hole injection, hot electrons, normally-OFF (NOF), normally-ON (NON), power switching, recovery, surface trapping.**

I. Introduction

GALLIUM nitride (GaN)-based high electron mobility transistors (HEMTs) are promising devices for power applications thanks to its superior material properties. The wide bandgap gives a high breakdown field, the ability to form a heterojunction leads to a high electron mobility and carrier density, as well as the low gate capacitance results in small switching losses, to name only few of them [1]. The development toward the usage of p-doped GaN at the gate enables the possibility of normally-OFF (NOF) operation, which is crucial for safety reasons. These HEMTs, which are called gate injection transistors (GITs), inject holes from the p-GaN gate resulting in an increase of drain current, often referred to as conductivity modulation [2]. One of the major issues of GaN HEMTs is the increase of dynamic ON-resistance $R_{ON,dyn}$ when the device returns from various kind of "stress" conditions to the ON-state. While OFF-state stress [3] and semi-ON state stress (i.e., simultaneous application of high voltage and moderate current) [4] are relevant stress conditions in operation, back-gating [5]–[9] is a condition mainly used for characterization purposes.

The increase of dynamic R_{ON} in NOF GITs is considered to be due to charge accumulation in the buffer [10], at the AlGaN surface [11], or both [12]. However, one cannot distinguish between buffer and surface trapping easily and so the topic is still under debate. For example, the buffer origin of negative trapped charge has been suggested only indirectly on the basis of thermal activation energy similarity to carbon defects [7], [10]. Additionally, no clear trend in the values of recovery time constants related to buffer and surface trapping can be recognized from thermal recovery. Furthermore, the recovery due to hole injection from forward gate current has also been observed, but no conclusion regarding the location has been made [13], [14].

Buffer charging can be unambiguously identified by means of back-gating measurements, initially proposed for NON devices [5]–[8]. Using back-gating measurements and signatures of thermal activation of recovery transients Bisi *et al.* [7] and [8] were able to distinguish between buffer and surface traps. However, activation energies in carbon-doped GaN might not primarily be referred to capture and emission processes, but can rather depend on the transport of charges [15], [16]. Moreover, in literature activation energies

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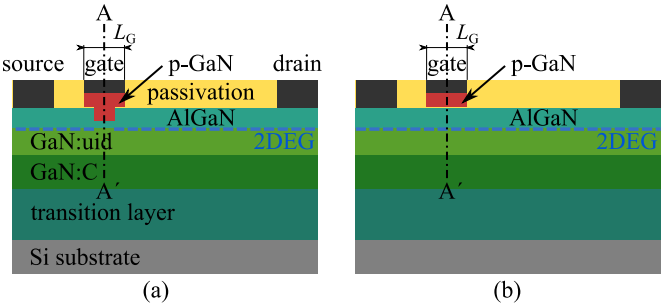

Fig. 1. Schematic cross sections of (a) NOF and (b) NON GITs. The gate length L_G of both device types is the same.

between 0.4 and 1.1 eV can be found for carbon-doped buffers [15], which allows for a very large range of dynamic effects to be falsely related to carbon defects.

It is important to point out that for studying the gate-bias induced recovery in NOF GIT devices the drain current transients can only be measured when a sufficiently high positive gate voltage is applied. However, the application of gate voltages above the turn-ON voltage of the gate diode speeds up the recovery, i.e., shortens the time constant of recovery transients [13], [14]. In turn, fast recovery processes become difficult to measure in NOF devices. In order to enable transient recovery measurements without hole injection, p-GaN devices with the same epitaxial growth, but with normally-ON (NON) behavior can be used.

In this article, we use specific fingerprints of the gate-voltage dependence of recovery time constants to clearly distinguish between stress-induced buffer and surface trapping in p-GaN GITs. We use specially fabricated NON GIT structures to enable back-gating measurements necessary to unambiguously identify buffer trapping. Using this approach, it has been found that OFF-state stress leads to negative charging of the buffer. When the device is subjected to semi-ON state stress, besides buffer trapping also surface trapping is identified. Even if our conclusions are similar to those of Bisi *et al.* [7] and [8], our proposed technique to distinguish between buffer and surface trapping uses the gate-voltage dependence instead of the temperature dependence of the recovery. Therefore, it is more general and also applies for highly carbon-doped layers, in which trapping/detrapping is limited by transport processes [15], [16]. Additionally, it is more direct, faster, and easier to interpret. Furthermore, the suggested technique is used on NON GITs instead of NON metal–insulator–semiconductor (MIS)-HEMTs as in [7], [8], and [17].

II. Experimental Details

A. Devices and Basic Characterization

In Fig. 1, the schematic cross sections of conventional (a) normally-OFF (NOF) [2] and (b) normally-ON (NON) gate injection transistors (GITs) are illustrated. In NOF devices a part of the thick AlGaN barrier below the gate is recessed and subsequently a thin AlGaN layer is regrown, which determines the AlGaN barrier thickness at the gate [18]. In NON devices

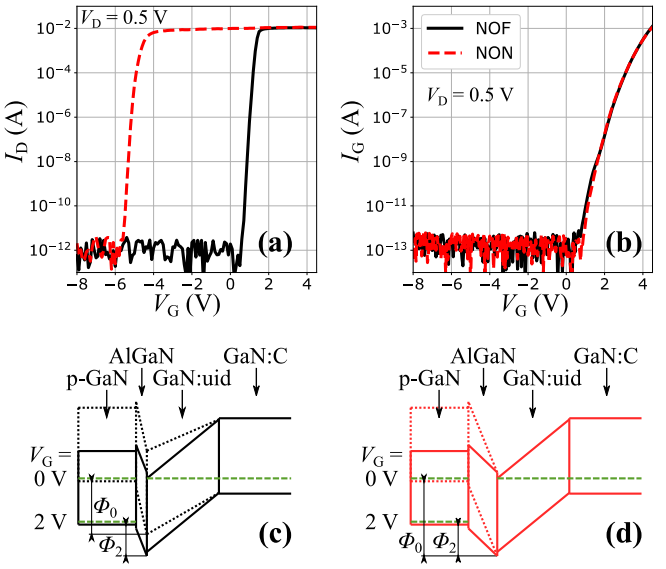

Fig. 2. (a) I_D–V_G and (b) I_G–V_G characteristics of NOF and NON GITs. Schematic band diagrams of the p-GaN gate structure along line A-A' (cf. Fig. 1) for (c) NOF and (d) NON device for $V_G = 0$ and 2 V. The barrier heights for hole transport Φ_0 and Φ_2 at respective $V_G = 0$ and 2 V are indicated.

instead, the recess step is skipped, which leads to a thick AlGaN barrier along the whole cross section of the device.

The GaN stack is epitaxially grown by metal-organic chemical vapor deposition (MOCVD) on a silicon (Si) substrate, which contains an approximately 2-μm thick transition layer (TL), an approximately 1-μm carbon-doped buffer layer (GaN:C) with a carbon concentration of roughly 10^{19} cm^{-3}, and an approximately 400 nm unintentionally doped GaN (GaN:uid) channel. The p-GaN epitaxial gate is contacted by an ohmic contact. The used test structures have a gate width of roughly 200 μm and a gate to drain spacing of 10 μm.

Fig. 2(a) and (b) shows the transfer characteristic (I_D–V_G) and gate–source diode characteristic (I_G–V_G), respectively.

The threshold voltage of the NON GIT is V_{TH}(NON) = −4.8 V, while it is V_{TH}(NOF) = 1.2 V for the NOF GIT (defined for I_D = 300 μA). The I_G–V_G curves are almost identical for both device types except the region below V_{TH}(NOF) where the gate current for the NOF GIT is slightly higher. Due to the gate-stack design, I_G of the NOF GIT is composed of two components: a component of the recessed part and a component of the non-recessed part (the latter is proportional to I_G of the NON GIT). These components share nearly the same area, so the difference between I_G of NON and NOF device is intrinsically small. The nuances in I_G are explained on the basis of band diagrams for recessed [see Fig. 2(c)] and non-recessed parts [see Fig. 2(d)] for V_G biases 0 and 2 V below and above V_{TH}(NOF). I_G is assumed to be to a large part due to hole current, which is determined by the barrier height Φ between the valence band maxima of the p-GaN layer and the AlGaN barrier. For $V_G < V_{TH}$(NOF) the barrier for holes in the NOF structure [see Fig. 2(c), dotted band diagram, barrier Φ_0] is lower than in the NON structure [see Fig. 2(d)] because no two-dimensional electron gas (2DEG)

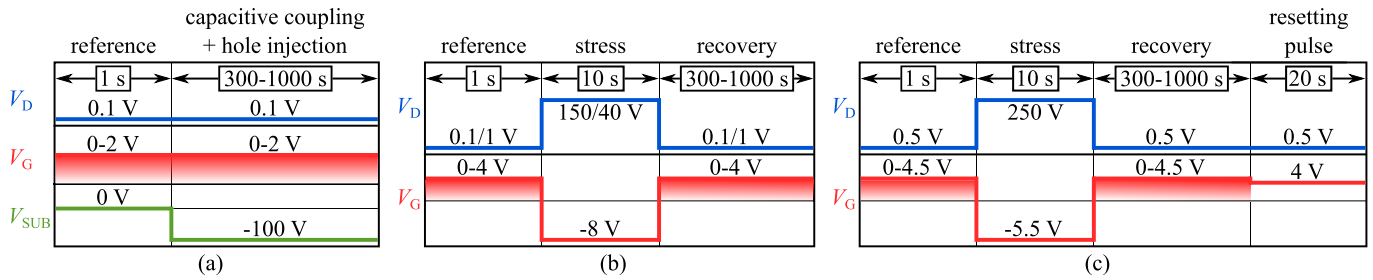

Fig. 3. Measurement sequences of (a) back-gating, (b) OFF-state stress, and (c) semi-ON state stress. For (b) and (c) $V_{SUB} = 0$ V.

is formed below the recessed p-GaN gate and the AlGaN/GaN interface is not pinned at the Fermi level. This leads to a slightly higher I_G in the NOF GIT in this regime, which agrees with the measurement in Fig. 2(b). On the other hand, for $V_G > V_{TH}$(NOF) the 2DEG is established also in the NOF GIT and the barrier for holes Φ_2 is the same for both device types leading to the same I_G. To sum up, besides nuances of I_G below V_{TH}(NOF), empirical measurements show almost identical gate diode characteristics for the NON and NOF device, which implicates the same number of injected holes from the p-GaN gate at a certain gate voltage V_G.

B. Measurement Setups and Sequences

Back-gating and OFF-state stress measurements were performed using Keithley 2636B source measurement units (SMUs). The time resolution of measurements in the used setup configuration is approximately 40 ms. For semi-ON state stress measurements additionally a Keithley 2657A high-voltage SMU and a Keithley 8020 protection unit were used, which leads to a time resolution of approximately 400 ms. The OFF-state stress measurement with $V_{D,str} = 40$ V was performed using a Keithley 4225 pulsed measurement unit (PMU), which has a voltage limitation of 40 V but allows to extend the timing of the first measurement datapoint in the short time range to 10 μs. We mention, that the PMU setup could not be used for fast back-gating measurements as it has only two different channels and for back-gating three channels are required.

Back-gating measurements are performed on NON GITs applying the measurement sequence depicted in Fig. 3(a) containing:

1) reference-phase (drain voltage $V_D = 0.1$ V, gate voltage $V_G = 0$–2 V, and substrate voltage $V_{SUB} = 0$ V), where the initial drain current $I_{D,0}$ is measured for 1 s serving as reference before stress;

2) "capacitive coupling + hole injection"-phase ($V_D = 0.1$ V, $V_G = 0$–2 V, and $V_{SUB} = -100$ V for a duration of 300–1000 s), where the 2DEG concentration decrease due to, e.g., capacitive coupling effect as well as its increase due to hole injection from the gate occur during the same phase. This allows the investigation of the hole accumulation process within the GaN buffer, which compensates the 2DEG depletion induced by the negative voltage at the substrate. More details are provided later in Section III.

Furthermore, OFF-state and semi-ON state stress are performed on NON GITs using the measurement-stress-measurement (MSM) technique [19], [20]. The measurement sequence for OFF-state stress is depicted in Fig. 3(b) and is composed of:

1) reference-phase ($V_D = 0.1$ V/1 V and $V_G = 0$–4 V);

2) stress-phase ($V_{D,str} = 150$ V/40 V depending on the instrument selection described above and $V_{G,str} = -8$ V for a duration of 10 s), where the 2DEG is depleted due to negative charge accumulation;

3) recovery-phase ($V_D = 0.1$ V/1 V and $V_G = 0$–4 V for a duration of 300–1000 s), for $V_G \geq 0.7$ V [see Fig. 2(b)] holes are injected from the p-GaN gate and accelerate the recovery of trapped negative charge.

The measurement sequence of semi-ON state stress is shown in Fig. 3(c) and contains:

1) reference-phase ($V_D = 0.5$ V and $V_G = 0$–4.5 V);

2) stress-phase ($V_{D,str} = 250$ V and $V_{G,str} = -5.5$ V for a duration of 10 s);

3) recovery-phase ($V_D = 0.5$ V and $V_G = 0$–4.5 V for a duration of 300–1000 s);

4) resetting pulse ($V_D = 0.5$ V and $V_G = 4$ V for a duration of 20 s), in order to bring the device back to its initial state, since full recovery of trapped negative charge cannot be achieved for low V_G values.

Finally, as comparison, semi-ON state stress measurements are also performed on the NOF GIT, where the stress condition is $V_{D,str} = 250$ V and $V_{G,str} = 1.2$ V. V_G in the recovery-phase is varied between 3 and 4.5 V, since for $V_G < 2$ V the device is not fully in ON-state and consequently the ON-current cannot be measured correctly [see $I_D - V_G$ characteristic in Fig. 2(a)].

V_D values between 0.1 and 1 V were used for measuring the recovery transients at different setup configurations to optimize the interplay of a small lateral electric field in the device and a high measurement resolution of I_D.

During semi-ON state stress $V_{G,str}$ values in the vicinity of the threshold voltage V_{TH} of the devices were used, which give a maximum stress current of approximately 300 μA. We limited the current in order to have negligible self-heating effects. We chose $V_{D,str} = 150$ V for OFF-state stress and $V_{D,str} = 250$ V for semi-ON state stress because under these conditions the largest decrease of I_D is observed [21]. Similar maximum I_D degradation at OFF-state stress for comparable drain voltages are observed by Uren *et al.* [22]. Additionally, it is important to point out that the used conditions for semi-ON state stress are not present under typical operational conditions.

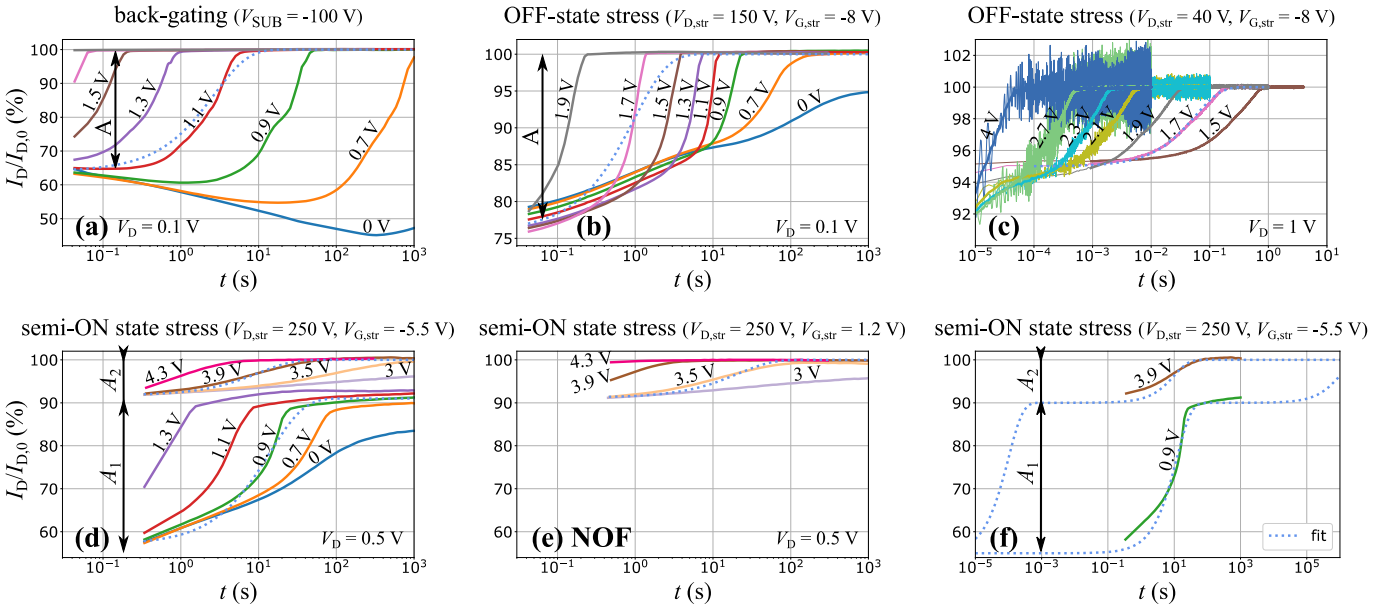

Fig. 4. Gate-voltage dependent normalized drain current transients $I_D/I_{D,0}$ of (a) back-gating ("capacitive coupling + hole injection"-phase) and recovery-phases after (b) OFF-state stress, (c) OFF-state stress with the pulsed setup, (d) semi-ON state stress for the NON GIT, and (e) semi-ON state stress for the NOF GIT. The dotted lines in (a)–(c) and (e) indicate fitted data using (1). In (f) fitting (dotted lines) of the original data from (d) (solid lines) in a larger time span for two different V_G values using a double-exponential function of (2) is shown. Fitting parameters for 0.9 V: $\tau_{semi-ON,1}$ = 12 s and $\tau_{semi-ON,2} = 10^6$ s, and for 3.9 V: $\tau_{semi-ON,1} = 10^{-4}$ s and $\tau_{semi-ON,2}$ = 10 s; degradation amplitudes: A_1 = 35% and A_2 = 10%.

The stress times used for this study are 10 s, while in typical switching operations the semi-ON state stress duration per switching cycle is only a fraction of this. Consequently, the degradation level observed in this study cannot encounter under normal conditions. Therefore, the degradation under switching conditions cannot be directly estimated from these experiments.

III. Results and Discussion

The V_G-dependence of normalized drain current transients $I_D/I_{D,0}$ of the "capacitive coupling + hole injection"-phase of back-gating and the recovery-phases after OFF-state and semi-ON state stress are shown in Fig. 4.

Focusing on the $V_G = 0$ V transient in the back-gating experiment [see Fig. 4(a)], the application of a negative substrate bias of $V_{SUB} = -100$ V causes an immediate reduction of I_D by approximately 35% at 40 ms. This is due to depletion of the 2DEG caused by the capacitive coupling effect [22], [23]. Afterward, a further decrease of I_D until $t \approx 300$ s is observed, which is referred to charge redistribution in the GaN:C layer within the defect band driven by the vertical electric field [24]. Positive charges propagate to the bottom of GaN:C leaving behind negative charged carbon acceptors, which leads to a further depletion of the 2DEG [25]. After 300 s I_D increases again, which is attributed to positive charge accumulation due to vertical leakage current through GaN:uid [22], [23], [26]. Wach *et al.* [23] and Karboyan *et al.* [26] have reported that holes can propagate vertically by extended defects from the channel region toward the buffer. The recovery at $V_G = 0$ V, i.e., pure thermal recovery, has been studied in [7]–[9] and [25]. In contrast, in this article, we investigate the hole-induced recovery due to gate current. With an additional injection of holes from the p-GaN gate by using gate voltages $V_G \geq 0.7$ V, we observe shortening of recovery time constants [see Fig. 4(a)]. It means, that the process of positive charge accumulation gets dominant and full recovery of I_D can be reached within the measured time window. A higher value of V_G leads to a higher hole injection rate and therefore to shorter times to reach the initial value $I_{D,0}$, i.e., initial electron concentration of the 2DEG.

Fig. 5 schematically illustrates all considered back-gating processes by means of band diagrams. Fig. 5(a) depicts the initial condition of a HEMT. The blue dot and its size represent the number of electrons in the 2DEG. By biasing the substrate in Fig. 5(b), the potential is raised, which immediately decreases the 2DEG density. The additional depletion originating from charge redistribution in GaN:C is referred to as process 1. The reduction of I_D back to its initial value can be compensated by positive charge accumulation either by leakage through the GaN:uid layer or by forward biasing the p-GaN gate, i.e., active injection of holes into the buffer (process 2). For example, from the $I_D(t)$ transient at $V_G = 1.1$ V in Fig. 4(a) it becomes obvious that the full recovery of the 2DEG concentration occurs within 10 s. The band diagram for such a steady-state situation, where the accumulated positive charges in the buffer shield the substrate bias, is shown in Fig. 5(c).

Although the recovery process in Fig. 4(a) is not fully exponential, an exponential approximation is used to compare time constants τ for different V_G values

$$\frac{I_D(t)}{I_{D,0}} = 1 - A \exp\left(-\frac{t}{\tau}\right) \tag{1}$$

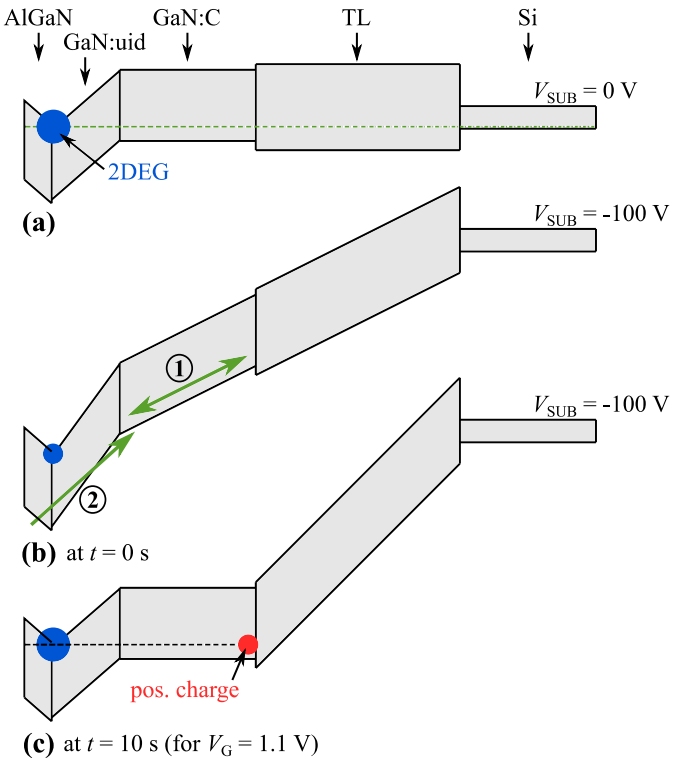

Fig. 5. Schematic band diagrams during back-gating indicating (a) initial condition ($V_{SUB} = 0$ V), (b) $V_{SUB} = -100$ V at $t = 0$ s, and (c) after 10 s, considering $V_G = 1.1$ V, when holes have accumulated in the GaN buffer and the initial 2DEG concentration is established again. The size of the blue dot represents the number of electrons in the 2DEG, whereas the red dot shows the position of accumulated positive charges. The processes denoted by 1 and 2 illustrate the charge redistribution in GaN:C and the hole injection from p-GaN gate into the buffer, respectively.

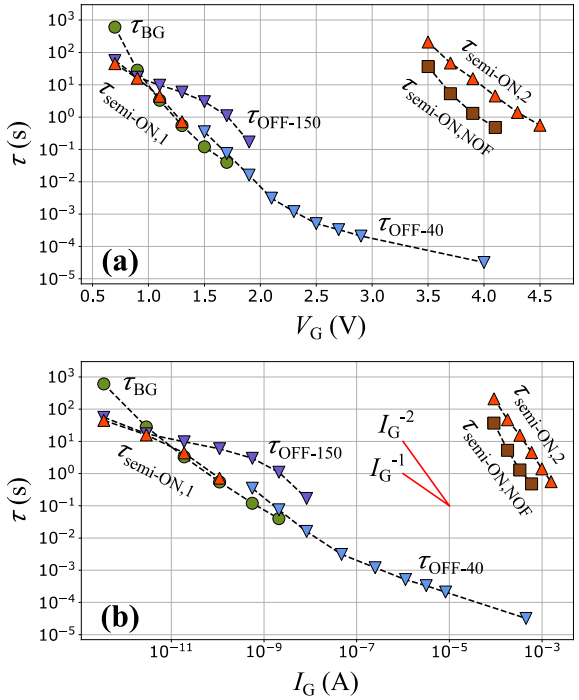

Fig. 6. Extracted time constants τ as a function of (a) gate voltage V_G and (b) gate current I_G from the data of Fig. 4 for back-gating (τ_{BG}), OFF-state stress ($\tau_{OFF-150}$, τ_{OFF-40}), semi-ON state stress ($\tau_{semi-ON,1}$, $\tau_{semi-ON,2}$) for the NON GIT, and semi-ON state stress for the NOF GIT ($\tau_{semi-ON,NOF}$). I_G values were extracted from the gate diode characteristic in Fig. 2(b). In addition, the slopes $1/I_G$ and $1/I_G^2$ are given in (b) as a comparison.

where A is the amplitude of I_D degradation, which is around 35% [see Fig. 4(a)]. An exponential fit of the data with $V_G = 1.1$ V is included by a dotted line. The extracted time constants of the back-gating measurement from Fig. 4(a) as a function of V_G and I_G are plotted in Fig. 6(a) and (b), respectively, and labeled as "τ_{BG}."

From Fig. 4(a) it becomes also clear that back-gating experiments would not provide useful results in NOF GITs. The minimum V_G to get a measurable I_D for transient detection in the NOF device is around 2 V. However, at this gate voltage, the high hole injection would fully recover the buffer before the first datapoint of the recovery transient is recorded.

The normalized recovery transients for different V_G after OFF-state stress on NON GITs with $V_{G,str} = -8$ V and $V_{D,str} = 150$ and 40 V are given in respective Fig. 4(b) and (c). The I_D transient for $V_G = 0$ V in Fig. 4(b) shows the recovery which is logarithmically evolving with time and is tentatively attributed to both, charge redistribution in the buffer and thermal recovery of accumulated negative charge. For $V_G \geq 0.7$ V the recovery is dominated by the injected holes from the p-GaN gate. Again, a larger hole injection leads to a faster recovery of I_D, and consequently to full recovery of the device within the measured time window.

In the measurements in Fig. 4(c) the pulsed measurement setup was used, which enables to capture the I_D transients at higher V_G values with a better time resolution. The trade-off is the larger noise for $t < 10$ ms due to shorter integration time, which can be, however, reduced by moving averaging (raw data are in thin, averaged data in thicker lines).

The drain current transients in Fig. 4(b) and (c) are approximated by the exponential function with a single time constant according to (1). Even if the transients in Fig. 4(b) for $0.9 \text{ V} \leq V_G < 2$ V vary faster than exponentially (compare the exponential fit by dotted line with the data for $V_G = 1.7$ V), the extracted time constants are not affected much. Indeed, stretched exponential functions were previously used for the time constant determination [27]. The I_D degradation amplitudes are around 22% for $V_{D,str} = 150$ V and 5% for $V_{D,str} = 40$ V. The extracted time constants as a function of V_G and I_G are given in Fig. 6(a) and (b), respectively, and labeled as "$\tau_{OFF-150}$" and "τ_{OFF-40}." There is a short V_G interval (1.5–1.9 V) where these two datasets overlap, showing the data consistency from the two setups. Most importantly, the $\tau_{OFF-150}$ and τ_{OFF-40} values in the interval $0.7 \text{ V} \leq V_G \leq 1.7$ V are close to those from the back-gating (τ_{BG}). Consequently, we suggest that charging processes at OFF-state stress are related to carbon acceptors in the buffer of the device. Indeed, the recovery process due to hole injection after OFF-state stress and during back-gating have the same physical principle: shielding of buffer potential by hole injection in it, thus recovering initial 2DEG concentration. Remarkably, the recovery time constants as short as 10^{-4} s [see τ_{OFF-40} at 4 V in Fig. 6(a)] have never been previously attributed to processes in the buffer.

For OFF-state stress we consider that buffer charging takes mainly place in the gate–drain access region and more particularly, closer to the drain side. For back-gating on the other hand the entire source-to-drain region is involved. For recovery, holes have to be injected from the gate to the buffer but then also propagate laterally toward the drain. The fast recoveries could hint toward the existence of a lateral hole conduction channel, e.g., two-dimensional hole gas (2DHG) at the GaN:C/TL interface [28].

The normalized I_D transients for different V_G after semi-ON state stress with $V_{D,str} = 250$ V and $V_{G,str} = -5.5$ V for the NON device are shown in Fig. 4(d). For $V_G < 2$ V the recovery saturates at around 90% of $I_{D,0}$. For significantly higher V_G values (≥ 3 V) the remaining approximately 10% recover within the measured time window. The higher V_G the faster the recovery. The recovery transient can be approximated by the following double-exponential function:

$$\frac{I_D(t)}{I_{D,0}} = 1 - A_1 \exp\left(-\frac{t}{\tau_1}\right) - A_2 \exp\left(-\frac{t}{\tau_2}\right) \quad (2)$$

where A_1 [$\sim$35%, see Fig. 4(d)] and A_2 ($\sim$10%) are the degradation amplitudes for the respective exponential transients with time constants τ_1 and τ_2 ($\tau_1 < \tau_2$). The extracted time constants as a function of V_G and I_G are plotted in Fig. 6(a) and (b), respectively, and labeled as "$\tau_{semi-ON,1}$" and "$\tau_{semi-ON,2}$."

Remarkably, the $\tau_{semi-ON,1}(V_G)$-dependence and $\tau_{BG}(V_G)$, $\tau_{OFF-150}(V_G)$, $\tau_{OFF-40}(V_G)$-dependences overlap well in the $0.7 \leq V_G < 1.5$ V range. This allows us to conclude that recovery processes with time constant $\tau_{semi-ON,1}$ are related to the buffer. In contrast, the $\tau_{semi-ON,2}(V_G)$-dependence is well separated from the $\tau_{BG}(V_G)$, $\tau_{OFF\text{-}150}(V_G)$, $\tau_{OFF\text{-}40}(V_G)$, and $\tau_{semi-ON,1}(V_G)$-dependences. Accordingly, we attribute the recovery processes related to $\tau_{semi-ON,2}$ to another trap location, most likely in the AlGaN barrier or AlGaN/SiN interface (referred here as surface). Former studies have shown that during semi-ON state stress hot electrons can accumulate at the surface [11], [13].

Fig. 4(f) shows the fitting of recovery data for $V_G = 0.9$ and 3.9 V from Fig. 4(d) using (2) over 11 orders of magnitude in time. The $\tau_{semi-ON,2}$ value for $V_G = 0.9$ V is extrapolated to nearly 10^6 s. For $\tau_{semi-ON,1}$ at $V_G = 3.9$ V the interpolated value of $\tau_{OFF\text{-}40}$ was considered. A double-step behavior is clearly seen in this expanded time scale. The simulation shows that in order to see the recovery behavior at both locations during a single time window, an equipment covering more than seven orders of magnitude in time is necessary.

Finally, the recovery transients after semi-ON state stress with $V_{D,str} = 250$ V and $V_{G,str} = 1.2$ V for the NOF GIT [see Fig. 4(e)] were measured for $V_G \geq 3$ V. For $V_G < 2$ V the device is not fully in ON-state and therefore buffer trap recoveries cannot be investigated. The extracted time constants for the NOF GIT as a function of V_G and I_G are plotted in Fig. 6(a) and (b), respectively, and labeled as "$\tau_{semi-ON,NOF}$." The $\tau_{semi-ON,NOF}(V_G)$-dependence overlaps with the $\tau_{semi-ON,2}(V_G)$-dependence for the NON GIT, suggesting that the recovery transients in NOF GIT are due to surface trapping.

Fig. 6(a) clearly shows that independent of the stress types the recovery processes related to buffer traps follow the same V_G-dependence (see τ_{BG}, $\tau_{OFF\text{-}150}$, $\tau_{OFF\text{-}40}$, and $\tau_{semi-ON,1}$) and have been observed in a time range of 10^{-4} to 100 s. $\tau_{semi-ON,2}(V_G)$ and $\tau_{semi-ON,NOF}(V_G)$ are well separated, suggesting the recovery cannot be done by hole injection into the buffer. For $V_G \geq 3$ V in the NON GIT, the buffer recovery would take approximately 10^{-4} s. Instead, in this V_G range, the recovery takes at least four orders of magnitude longer and is related to trapping above the 2DEG, i.e., to the surface. Indeed, during semi-ON state stress, hot electrons have sufficiently high energies to overcome the AlGaN barrier and reach the surface [11], [13]. The much longer hole-induced recovery of surface state can be related to: 1) more complex path the holes pass on their way from the gate to the surface compared to the bulk and/or 2) high hole capture cross section on surface traps due to their large lattice relaxations [29], [30]. Further investigations, also about the nature of surface states involved, are necessary to answer this question.

A difference between the recovery mechanism of the buffer and the surface can also be recognized in terms of different slopes of the $\tau(I_G)$ distribution in Fig. 6(b). While $\tau(I_G)$ of the buffer approximately goes with $1/I_G$, it rather follows $1/I_G^2$ for the surface. However, the underlying phenomenon is not understood yet and out of the scope of this publication.

We would like to emphasize the unique feature of NON compared to NOF GITs with respect to trap identification and localization. Since the NON GIT device can be in the ON-state without injecting holes from the p-GaN gate, lower V_G can be used to detect the relatively fast recovering buffer traps. For the NOF device this is not possible because V_G values larger than 2 V are required for measuring I_D in ON-state. In Fig. 6(a) for $V_G \geq 3$ V, one can see that the buffer recovers within approximately 10^{-4} s, which is faster than most common measurement setups can resolve. Consequently, analysis of dynamic R_{ON} measurements has to be treated cautiously: If the measurement resolution of the used setup is not sufficiently fast, one might falsely assume that dynamic R_{ON} is relevant only after semi-ON state stress as this is the only bias condition, in which surface trapping occurs. However, in reality, the dynamic R_{ON} increase due to buffer trapping is just not observed. Therefore, real dynamic R_{ON} might be far higher, for both, semi-ON state and OFF-state stress but particularly for the latter. Even if the buffer and surface recovery for a single V_G value cannot be revealed during a single transient [compare measurements in Fig. 4(d) with simulations in Fig. 4(f)], it is still possible to distinguish between those two processes thanks to their specific $\tau(V_G)$-dependence.

IV. Conclusion

In this article, we make a step forward in understanding the location of the negative accumulated charges in GaN GITs submitted to OFF-state and semi-ON state stress. By comparing the V_G-dependences of related recovery time constants with those of back-gating experiments in NON GITs we are able to distinguish between the recovery processes in the buffer and at another location, likely at the AlGaN barrier/SiN passivation

interface (i.e., surface). It is found that the OFF-state stress causes only charge trapping in the buffer. On the other hand, semi-ON state stress leads to both, trapping in the buffer and at the surface.

Furthermore, NON structures allow the investigation of gate-dependent recovery processes in the buffer in unprecedently large time ranges between 10^{-4} and 100 s which is not possible in standard NOF devices. In NOF devices only the response of slow surface traps is measurable, since due to larger hole injection at higher required V_G, the response of buffer traps is too fast and not resolvable by most commonly used equipment.

Finally, our approach to distinguish between buffer and surface traps based on $\tau(V_G)$ comparison is simple, straightforward and does not need time-consuming temperature-dependent measurements. Moreover, the effect of buffer and surface traps on I_D can be characterized by respective coefficients A_1 and A_2 in (2), which can be used for technology and epitaxial material optimization.

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