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Review

Reconfigurable field effect transistors: A technology enablers perspective

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ABSTRACT

With classical scaling of CMOS transistors according to Dennard's scaling rules running out of steam, new possibilities to increase the functionality of an integrated circuit at a given footprint are becoming more and more desirable. Among these approaches the possibility to reconfigure the functionality of a transistor on the single devices level stand out, as by such an approach the same physical circuitry is enabled to perform different tasks in different configurations of the circuit. Reconfigurable transistors that allow the reconfiguration from a p-channel to an n-channel transistor and vice versa have emerged as an important example of such devices. The basic concepts required to built such devices have been proposed more then 20 years ago and the field has continuously developed ever since. In this article first the basic classification of reconfigurable field effect transistors is reviewed an described form a new angle. In the second part the important technology enablers to construct reconfigure field effect transistors are examined. Further the historical development, starting at the proposal of the main concepts up to the current status of device and circuit development are described. The most important additional features that have been introduced in the last years in order to even further increase the flexibility of the devices are discussed. Finally the application potential of reconfigurable transistors is described placing the spotlight on hardware security and neuromorphic applications.

1. Introduction

The reconfigurable field-effect transistor (RFET), is an electronic device whose conduction mechanism can be reversibly reconfigured between n-type and p-type operation modes [1]. To enable this functionality, those devices do not rely on chemical doping caused by impurities but rather on electrostatic doping, i.e. the generation of mobile carriers via an external potential. Depending on the bias, either electrons or holes are generated in a nominally intrinsic semiconductor. This concept has been reported under a variety of names, such as polarity control, dehancement FET, Schottky barrier biasing, or field-induced drain extension. Regardless of the name, those devices are usually controlled by at least two independent gate electrodes: one is used to select the kind of charge carrier (electrons or holes) and the second one modulates the channel conductance and so the amount of current. To this end, reconfigurable transistors combine the functionality usually realized by two different devices, in a single one. In comparison, a classical Field Effect Transistor (FET) is fixed to either n-type or p-type operation by the underlying fabrication process. The programming of RFETs, in contrast, can be done in a static fashion or dynamically reprogrammed at run-time. This transistor-level reconfigurability has the potential to overcome some of the fundamental limitations of conventional CMOS technologies. Introducing CMOS-compatible reconfigurable transistors as add-on functionality can increase the versatility of electronics systems without the need for scaling. Based on a higher level of logic expressiveness, reduced costs per basic implemented logic function are projected.

The remainder of this paper is organized as follows. First, we discuss a new angle of classifying the various RFET device concepts in Section 2. In Section 3 we break down the basic requirements for RFET fabrication into five simple requirements, which we call technology enablers, before we dive into the historic development from devices towards circuits in Section 4. In Section 5 we discuss value added features, which give the possibility to further enrich the RFETs functionality. We conclude our paper with an overview of the future applications of this emerging technology in Section 6 with a focus on the areas of hardware security and neuromorphic computing.

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2. Classification of RFET concepts

The term RFET includes a broad family of devices that enable a reconfiguration of the dominant carrier type. The most important concepts are based on either Schottky-barrier field-effect transistors (SB-FET) or band-to-band tunneling transistors (TFETs). In the first group, the transport is dominated by a tunneling process through the Schottky-barrier at a metal–semiconductor interface. Here, a doping-free channel in combination with a midgap metal electrode at source and drain is typically used to facilitate an relatively equal electron and hole transport, which can be selected by the applied bias conditions (Fig. 1). This feature has become known as polarity-control (PC). Further, multimode concepts have been proposed, which extend the concept of reconfigurability from polarity control to charge injection mechanism control. Device architectures combining TFET and SBFET have been proposed, as well as concepts combining either of these two with an impact ionization (IMOS) or negative-differential-resistance (NDR) mode. In principle all of these devices possess the feature of polarity-control, however, they might be optimized to favor one carrier type depending on the target application. All device concepts have in common, that they are composed of at least two independently controlled gate electrodes, where one, the so-called polarity gate (PG, historically often called program gate) controls the kind of carrier or transport mode, while the control gate (CG) switches the transistor on and off.

2.1. Schottky barrier-based approaches

A multitude of different RFET architectures and working principles based on intrinsic channels with Schottky barrier contacts have been proposed over time. Typically, they have been differentiated by the positioning of the program gates as well as the applied bias conditions. While this classification is still useful, we propose an alternative approach here, which is to group the devices by the transport mechanism induced with the steering gate (control gate). For this lead to only two group:

- Direct control of the carrier injection through and over the Schottky barrier [2–6]
- Control of the transport of previously injected carriers over a thermionic barrier [7–13].

All SB-RFETs can be attributed to either one or the other group, or provide both functionalities in one (Fig. 2). Further, there are devices, which combine one of these functionalities with a band-to-band-tunnel or impact ionization mode, as discussed later. Typically, all those devices are built on metal/intrinsic semiconductor/metal heterostructures. In the most simple version, a common back-gate reaching over the whole channel overlapping both Schottky barriers is used as a polarity gate (Fig. 2(d)).

Depending on the applied voltage sign, the polarity is set by bending the energy bands in the semiconductor. Since the back gate covers the whole structure, positive (negative) voltages allow the injection of electrons (holes) from both contacts into the entire channel. This concept is often referred to as electrostatic doping the device itself, albeit all concepts are somewhat utilize electrostatic doping. The top control gate modulates an additional energy barrier in the center of the channel switching the transistor on and off.

To simplify the structure and to provide a better gating control through potentially thinner oxides, the back gate can be replaced by two additional top gates placed above (Fig. 2(e)) or below (Fig. 2(f)) the Schottky junctions. By steering these two gates simultaneously as polarity gates with the same fixed voltage applied, one can control the type of carrier injected at the junctions while modulating the channel conductance through the control gate, placed like before in the middle of the device. Main benefit over the simple electrostatic doping concept (d) is that the gates do not compete with each other regarding the control of a certain channel region. As a result, it has proven to be operational at lower voltages. Also, the implementation simplifies the device fabrication as all gates are patterned from the front. It was shown that the same device structure can be operated in an impact ionization mode when V_{DD} is substantially increased above the bandgap energy of the channel material, leading to steep subthreshold swings below 60 mV/dec at

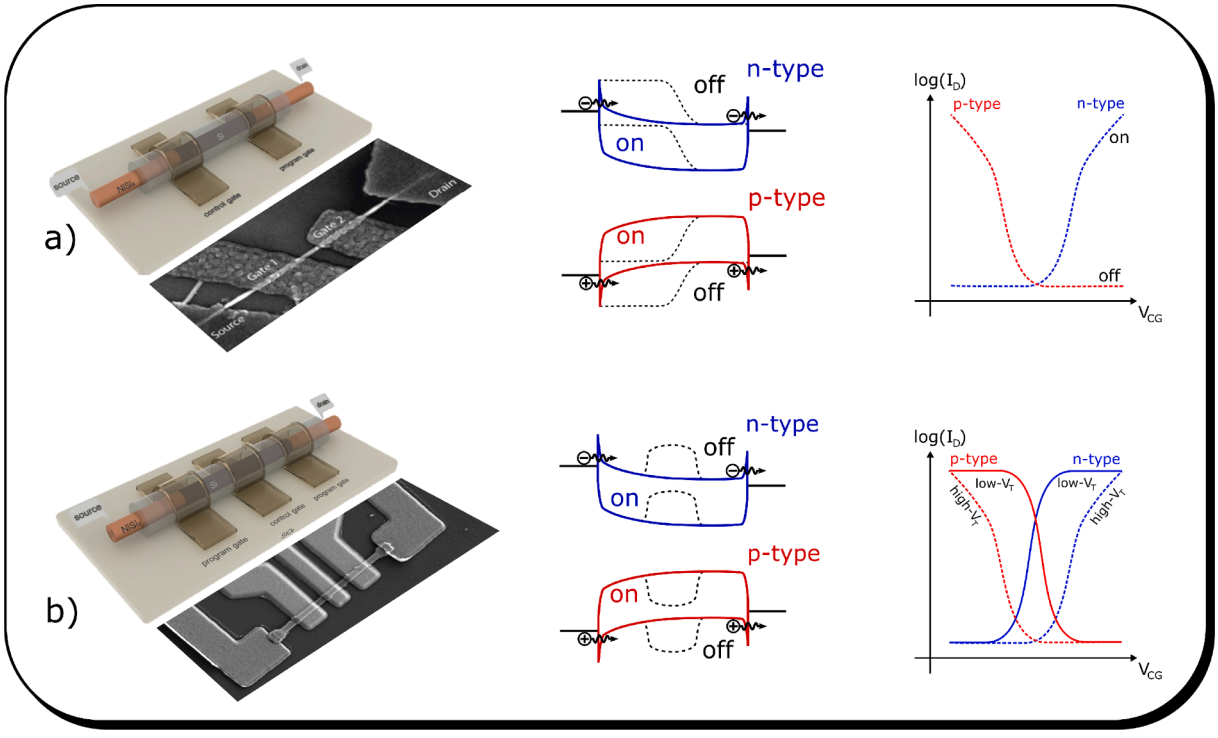

Fig. 1. Schematics, SEM images, band diagrams, and generic transfer characteristics of Schottky barrier based nanowire RFET. (a) Dual gated RFET with individual control at each barrier and (b) three-gated RFET with programming at both junctions simultaneously are shown.

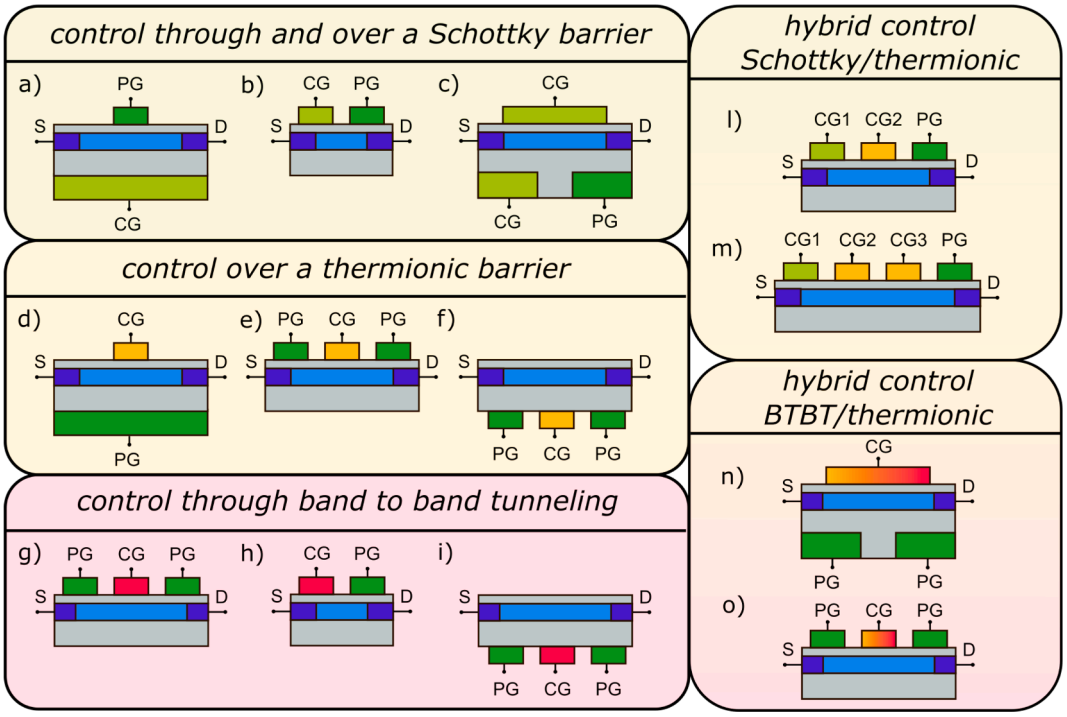

Fig. 2. Several RFET concepts, classified by the control mechanism employed. The program gate is always represented in darker green. (a-c) control at the Schottky barrier: here the control gates are always colored in light green. (d-f) control by raising/lowering a thermionic barrier: the control gates are in this case represented in yellow. (g-i) control through the enablement of a band to band tunneling phenomenon: the control gates are shown in dark red. (l,m) hybrid concept merging control through and over a Schottky barrier and over a thermionic barrier. (n,o) hybrid concepts of mixed band to band tunneling and thermionic control switching devices. Here a single control gate can trigger the switching on and off of the device through the two mechanisms depending on the electrostatic doping that is induced in the drain/source regions: for this reason, CGs are colored in both yellow and red.

room temperature [11]. Another version of the same structure is typically applied for 2-D layer materials, where all or some of the individual gates are carried out as buried-gates (Fig. 3(f)). Still, the control gate is tuning a thermionic barrier to control the current output of the device.

Interestingly, the same structure as employed for the concept in Fig.2 (d) can be also employed for a competing concept with ambipolar operation and selective carrier filter in the middle of the channel (Fig. 3 (a)). In this case the back gate is operated as control gate injecting both types of carriers into the channel depending on the applied voltage range. Thus the buried control gate provides an ambipolar behavior when steered, by directly tuning the Schottky barrier. The polarity gate placed at the top blocks the undesired charge carrier from passing through the whole channel. These two concepts may appear very similar, if not equivalent: in reality, the electrostatic doping concept does not have an ambipolar behavior since the polarity of the device is programmed directly at the Schottky junctions, while in the filtered ambipolar operation concept both carriers can be injected but one type is blocked in the middle of the channel by the band bending provided with the top polarity gate.

This difference gets especially obvious for structures where front and back gate are very similar in terms of size and oxide thickness, like employed for some 2-D based RFETs. Here, the underlying ambipolar characteristic is not suppressed by the polarity gate but rather shifted with respect to the source potential. This might be harmful in case of large voltage over and undershoots, which will turn the device on in the opposing direction. Also, an accumulation of the unwanted carriers inside the channel leads to high delay times during reprogramming. To prevent this effect, the concept with independent control of carrier injection (Fig. 2(b)) was invented. Typically, a dual gate structure is used; the polarity gate overlaps the drain-sided barrier and sets the polarity of the device by blocking the undesired carrier type directly at the barrier, while the control gate at the source-sided junction controls the carrier flow of the other carrier type through the channel. In this way the suppression of the ambipolar branch is executed directly at the Schottky contact preventing the injection of the unwanted carrier into the channel. A main benefit of this concept are the ultra-low off-currents, as the source-drain leakage is blocked directly at the Schottky barrier and not only by a thermionic barrier in the center of the channel. If both program and control gate are switched with respect to their alignment at source and drain, the ambipolar operation mode gets dominant again.

In a special version of this architecture for 2-D materials, the control gate is shared from both top- and bottom gates at the source side, while a single bottom gate is employed at the drain side (Fig. 2(c)). This three-gate structure increases the gate-control over the injecting barrier [14].

The benefits of the two basic concepts can be combined in a single device with three or more multiple independent gates. To achieve this, the three independent gates RFET (TIG-RFET) architecture (Fig. 2(l)), albeit structurally identical to Fig. 2(e), is programmed on the drain-sided barrier alone. The other two gates can be used to turn the transistor on or off. Depending on if the steering gate is aligned on top of the Schottky barrier (CG1) or at the center of the channel (CG2), the device acts as either the electrostatic SBB concept or the independent-injection-concept. The device can be seen as an 'all-or-nothing' function, passing a current only if all gates are biased to 0 or if all gates are biased to 1. This enables improved functionalities: for example, an wired-AND logic gate built over a single transistor has been demonstrated [15]. In addition, a steeper subthreshold slope is achieved with the middle gate concerning the source-sided gate. This is because the carriers are already injected through the Schottky barrier when the transistor switches, unlike in the previous concept where the switching was controlled directly at the junction by the only control gate. The option to combine both mechanisms in a single device can be exploited on the circuit level for power-saving techniques [16]. The number of gates can be increased as long as the resistance of the Schottky barrier is dominant as compared to the resistance of the channel (Fig. 2(m)) as discussed in [17].

2.2. Non-Schottky barrier approaches

Reconfigurable devices have also been proposed [18–20] exploiting band to band tunneling (BTBT) as the dominant conduction mechanism. Such devices are generally composed by two highly doped silicon regions separated by the nearly intrinsic channel region. By steering the two contact regions with sufficient voltages, it is possible to induce enough band bending to allow electrons to tunnel from the valence band of the p + doped contact region to the conduction band of the intrinsic region and thus to be collected at the other n + doped contact region.

In [18], a double gated structure is employed to steer the injection of carriers due to BTBT, while suppressing the intrinsic ambipolar behavior of the device itself. Therefore, one of the gates actually switches the device on and off, while the other one blocks the injection of the undesired polarity charge carriers, reducing in this way the ambipolar behaviour of the device. Reversing the gate voltages allows to switch the polarity of the device, realizing in this way a reconfigurable TFET. Since the conduction mechanism does not rely on thermally generated carriers and there is no Schottky barrier between the carriers reservoirs and the channel, lower sub-threshold swings are foreseen. This particular device however suffered from low values of on-current, making it slow during logic switching events. Also, the heavily doped contact regions are needed in order to obtain band to band tunneling. Yet, doping is harder to control on a nanoscale. These junctions differentiate the Tunnel-RFET from the SB-RFET, albeit in this case, two gates are employed. In any case, the result is again a transistor that shows unipolar n- or p-characteristics depending on how the two gates are steered.

RFET hybrid concepts combining both TFET and thermionic switching mechanisms (Fig. 2) were introduced in [21,22]. In these cases, additional gates steering the channel regions close to drain and source contacts, can induce electrostatic doping combinations that enable to program the device as an n-type/p-type TFET/thermionic switching device. Note, that there are also reconfigurable concepts based on single-electron-transistors, electron–hole bilayer transport, or spin-control, which are beyond the scope of this work.

3. Technology enablers

Independent of the chosen concept and working principle a set of five design and material key elements can be identified, which are needed to bring the RFET to a mature level. In this section we will reason about these so called technology enablers and review about the most important developments in this regard.

The first enabler is the presence of two or more independent gates. As already reviewed in section II, this feature deeply characterizes reconfigurable devices since the additional gate is needed to switch the device between operational modes. At the first glance, this is a drawback to classical MOSFETs, as a higher area is needed for the same amount of individual transistors. The main challenge associated with this feature is to turn this apparent drawback into a benefit in terms of functionality. For example, it has been shown, that XOR and Minority gates can be built with fewer amount of transistors and lower circuit level delay [23,24]. Dynamic reconfiguration between basic circuit functions like NAND and NOR can be achieved [25,26].

For three-gated structures, the concept of polarity-control has been extended to mode control, e.g. by exploiting the differences in threshold voltages of three-independent-gate devices for power saving techniques [27]. Impact ionization in combination with a positive feedback effect has been demonstrated to allow steep subthreshold slopes down to 6 mV/dec at an $V_{DS} = 5$ V, posing an interesting option for analog designers [11]. As a consequence, a comparison of device performance metrics alone is not sufficient to benchmark RFET technology. While the first enabler is more a design feature, most of the technology enablers are in close relation to material properties. During the early years, research on reconfigurable device concepts has been focused on one-dimensional (1D) nanostructures, such as carbon nanotubes [7], vapour-liquid–solid (VLS) grown silicon nanowires [4] and germanium nanowires [28]. Those materials provided a high surface quality and uniformity in very narrow structures making them the perfect candidate for early device demonstration.

The development was followed by a transition towards more industry-oriented platforms, such as top-down etched nanowires [8,9], FinFETs [11] or planar SOI-based FETs [29,30], which promise a CMOS co-integration. Also devices from poly-crystalline silicon have been realized [31–34]. While inferior in terms of pure performance measures they pose an option for back-end-of-line (BEOL) integration.

Germanium has been identified as a promising channel material towards the realization of RFETs with additional negative differential resistance capabilities [35,36] and with the prospects of enhancing speed and power efficiency of RFETs [28]. To allow for a deterministic top-down fabrication, Ge RFETs have also been realized with Ge on insulator (GeOI) wafers [37]. On the other hand, also two-dimensional

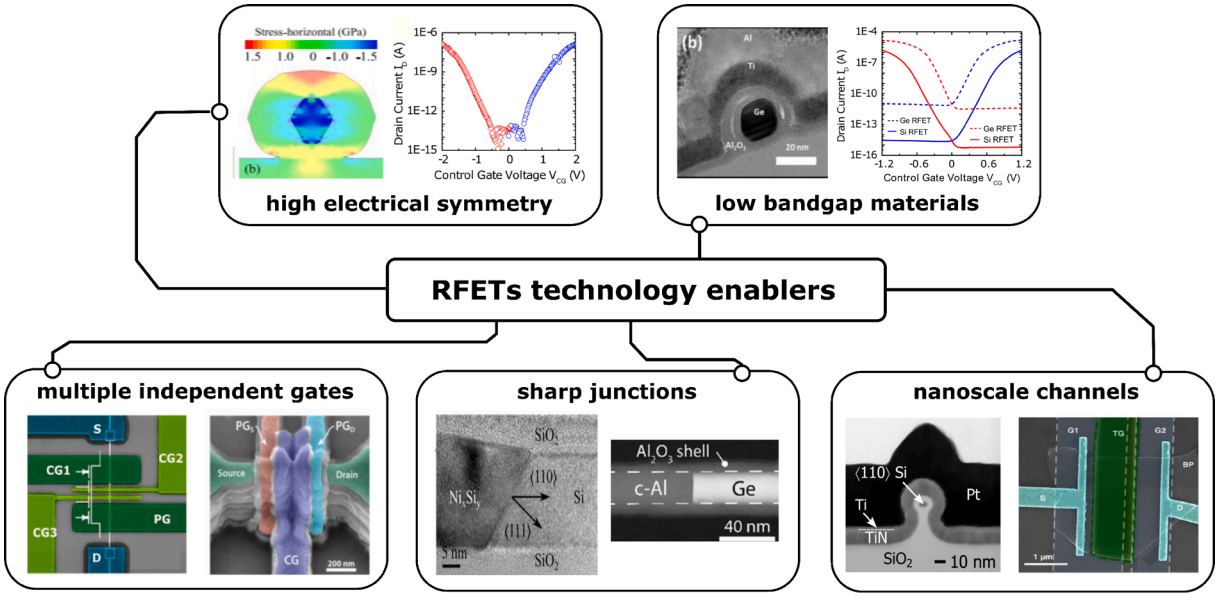

Fig. 3. Summary and visual exemplification of the five main technology enablers for successful RFET device fabrication, as discussed in the text.

(2D) layered systems, like graphene [13], dichalcogenides, e.g. WSe2 [12,38] or MoTe2 [39,40], and black phosphourous [14] have been put into the focus. These materials exhibit increased electrostatic control at high theoretically achievable current densities. Properties such as thickness-dependent band structures, closed dangling-bond free surfaces and stackability of different insulating, semiconducting and conducting 2D materials enable optimized realizations of such device concepts [41].

Beyond that, some demonstrators have also been shown on organic materials [42–44]. Here, the visioned applications are mainly in the area of flexible substrates. However, regardless of the material system used, organic RFETs still demand for more miniaturized channels with a better gate control to facilitate a high enough current density and reduced voltage demands.

Another enabler ensuring a high gate control are sharp junctions. For band-to-band tunneling based devices, a broad smeared-out potential gradient will lead to a thick tunnel barrier and thus a lower subthreshold slope. For Schottky-barrier based devices, sharp junctions are conveniently realized by the thermal formation of a metal silicides or germanides [45]. Such a silicidation process can from metal/semiconductor interface with up to atomic scale sharpness. In silicon based devices NiSi2 is very desirable in this regard, because it shares an epitaxial relation with Si. For the Ge material system monolithic Al-Ge-Al heterostructures pose a deterministic top-down fabrication platform enabling RFETs with a stable contact crystal phase and abrupt interfaces ensuring a reliable and reproducible contact formation [46]. If those contacts are intruded into a semiconductor nanowire or nanosheet, a gate contact placed at the junction can control the carrier injection with high precision. Technologically, the main challenge is the control the position where the silicide/germanide is formed with an high device-to-device uniformity [47,48].

Besides the location also the electrical properties of the contact has to be controlled. This is aggravated by the fact that most metal–semiconductor combinations show a high variety of phases, which have to be controlled. For channel materials not forming direct metalide contacts other solutions have to be found to realize sharp junctions. In 2-D materials this is often solved by placing the Source and Drain electrodes on-top of the channel, while the gates are buried below. This creates the need for a very thin back-gate dielectric to influence the injection within a reasonable low operation voltage.

Further, the application of RFETs in CMOS circuits demanded for the realization of equally large currents for electron and holes in both conduction modes. As both are facilitated by the same channel, individual optimization of widths and lengths for both device types as pursued in CMOS is not possible. We view this p-type to n-type symmetry as the final technology enabler, albeit its benefit is not obvious right on the device level. For example, having no symmetry in an inverter would shift the switching point away from $V_{DD}/2$ so that cascading of multiple stages of logic after one another would be hindered. This would be detrimental especially for highly-scaled electronics which should operate at a very low voltage level. Simon et al. have evaluated a number of different Si-based RFET concepts having the focus exactly on the aspect of symmetry [6].

Simultaneously, it is also important that the equal currents are provided by an equal set of applied drain, gate, and program voltages. This point is often overlooked in the early stage of device research. A high degree of symmetry has been mainly achieved for silicon devices so far, while all other channel materials are lacking in at least one of the criteria.

For silicon-based polarity-controllable devices, the main measure applied to yield symmetry is the midgap alignment of the source/drain contacts, like present in the NiSi2/Si material system. In addition, stress, e.g. induced by self-limiting oxidation, or Si3N4 layers can be a secondary effect to fine-tune the symmetry between electrons and holes currents [5,49]. Material systems that can not rely on the formation of thermally alloyed contacts have to find other measures to tune. For example combinations of metals with different work functions at source and drain have been proposed for current matching. Another approach is the use of two work function materials within the same gate to influence the shape of the blocking potential within the channel [10].

The need for a symmetric p- and n-type operation is also the driver for our last technology enabler. As an individual optimization of the transport for both carrier types is not possible, the channel material should be chosen in a way it supports both operation modes. In this regard, the use of low-bandgap materials, such as Ge or InAs, has been proposed to increase performance and especially to lower the threshold voltage. The injection of carriers via tunneling mechanisms at a given electric field increases with the use of materials with a comparatively low bandgap. For Schottky-barrier based devices, the performance gain is simply based on the fact that the combined barrier height for electrons and holes adds up to the bandgap value. On the other hand, one should also consider the off-state leakage currents, which tremendously increase with decreasing bandgap. Si-based solutions [4] still allow for the lowest I_{OFF} values due to its wider bandgap in comparison to Ge (Si: 1.12 eV; Ge: 0.66 eV). However, the special structure of RFETs blocking the undesired carrier type helps to alleviate this drawback for low-bandgap materials. Also the contact material can be tuned to yield a further effect. Germanium-based devices with Al-Ge contacts have shown a better off-state than its counterpart with Ni2Ge-Ge. This can be attributed to the strong Fermi-level pinning in the Al-Ge system close to the valence band.

Beyond group IV materials, Nakaharai et al. showed in 2012 that even graphene, despite the absence of a band gap, can be used to realize polarity control devices exploiting a double gate structure [13]. Also layered transition metal dichalcogenide (TMDC), such as $MoTe_2, WSe_2$ are supposed to yield a bandgap lower than silicon.

To sum up, the development of a powerful reconfigurable field effect transistor device, regardless of the exact layout or material system boils down to the use of those five technology enablers, Multiple Independent Gates, Nanoscale Channels, Sharp Junctions, High Electrical Symmetry, and Low Bandgap Materials.

4. From device research to circuit implementation

This section provides a short dip into the history of RFET research, illustrating how the research areas of RFET devices have extended over time. While 20 years ago predominately material and transport physics research have been conducted, the work has shifted more towards the circuit and system level over the last few years [50]. While there are still interesting research questions open on all levels, it is believed that this general trend will hold true.

4.1. From principles to devices

The roots of RFETs go back to the early 2000s when researchers from Taiwan's National Nano Device Laboratories and Institute of Electronics, National Chiao Tung University searched for a way to suppress the undesired high off-state currents in ambipolar Schottky Barrier Thin Film Transistors (TFTs). The solution they came up with was to create a device with two gates [51]: one, the control gate, is placed to directly gate the source-sided Schottky junction. This gate and the drain-sided Schottky junction are then covered by a thick oxide. On top of this, a sub gate (which today we would call polarity gate) is placed to cover the complete transistor. By this sub-gate, the undesired carrier injection from the drain-side in the off-state could be lowered by more than three orders of magnitude which resulted in on/off current-ratios as high as 10^6. While this first device was based on TFT technology with polycrystalline silicon [31], a later implementation was based on SIMOX wafers with monocrystalline silicon [52]. This device had an improved architecture achieving max–min current ratios up to 10^9 and subthreshold swings down to 61 mV/dec, but still needed a program voltage significantly higher than the operating voltage.

Even though these early reconfigurable FETs have been demonstrated for the first time, due to the very special target application the

potential of the technology had not been recognized in the scientific community. The concept was brought back to attention a couple of years later. Due to the continued scaling of device sizes according to Moore's Law, the stable and reliable operation of MOSFETs has been challenged by the nanoscale device dimensions. Doping by incorporation of chemical impurities became increasingly difficult for ultra-scaled technology nodes because of the increasing impact of dopant fluctuations and dopant deactivation in nanoscale channels [53,20]. As opposed to this, devices facilitating electrostatic doping promised potentially ultra-sharp junctions with well-controlled carrier concentration profiles and reduced defect density [54].

A team from IBM T.J. Watson Research Center realized a reconfigurable FET based on a carbon nanotube as channel material, having a single control gate at the top and a polarity gate covering the whole channel from the backside [7]. The program gate voltage is applied simultaneously at both Schottky junctions. Depending on the sign of the applied voltage, the polarity is set by bending the bands in the semiconducting channel region; a positive (negative) voltage allow the injection of electrons (holes) from both contacts into the entire channel. The top control gate modulates an additional thermionic energy barrier in the center of the channel switching the transistor on and off. Since the carriers are already injected through the Schottky barrier when the control gates operate, the device can achieve an ideal slope of 60 mV/dec at room temperature. Interestingly, the same structure can be also employed for a competing concept called ambipolar operation with selective carrier control [55,3]. In this case, the back gate is operated as a control gate injecting both types of carriers into the channel depending on the applied voltage range. Thus, the buried control gate provides an ambipolar behavior when used to steer the channel. The polarity gate placed at the top blocks the undesired charge carrier from passing through the whole channel. In 2008 this concept was improved by W.M. Weber and a team from Infineon, by exploiting a NiSi2/Si/NiSi2 heterostructure with thermally intruded silicide contacts [56]. In this way, a gate aligning directly at the drain-sided barrier was used to block the undesired carrier type [2]. The concept typically exhibits a higher subthreshold slope but a lower source-drain leakage. Until today, all Schottky barrier-based RFETs still rely on either of the two programming mechanisms (Fig. 2), or a combination of both.

4.2. From devices to logic gates

Following and improving the two basic mechanisms proposed, research groups have focused on 1D- nanostructures, predominantly silicon nanowires [4,8,9,57,5] in the following years. The name "Reconfigurable Field Effect Transistor" itself was first introduced by Heinzig et al. from NaMLab in 2012 [4], for an improved demonstrator of the concept with independent control of carrier injection (Fig. 2(b)). The device was refined just one year later, showing nearly perfect symmetry between n-type and p-type currents [5] which is a prerequisite for the efficient use of reconfigurability in CMOS-like circuits. This was achieved by employing oxidation-induced mechanical stress into the channel [58], enabling an operation with only two distinctive potentials, e.e. V_{DD} and ground. The operation was verified by demonstrating the first reconfigurable complementary inverter circuit [5]. In 2012 a research group at EPFL has shown that a three gated device with the two outer gates overlapping the Schottky junctions largely improves the concept of back-gate programming, lowering the programming voltage and simplifying process integration [8].

Simultaneously with these more sophisticated device demonstrators, the development of the first logic gates exploiting the reconfigurability started. In this regard, two major design paradigms can be distinguished in the literature at the logic optimization level to achieve more functionality per computational unit – implicit and explicit reconfigurability [59]. Explicit reconfigurability is realized in those circuits which can alter the functionality by an external signal on request. Here, a simple example is a NAND gate, which can be dynamically reprogrammed to NOR functionality when built from RFETs [60]. In contrast, implicit reconfigurability can be used in logic gates where a particular combination of inputs results in an electrical scenario that yields a truth table with a higher expressive capability. For example, exploiting three-gated RFETs, compact realizations of XOR and MAJ can be built using a lower number of transistors than in classical CMOS [8].

Ever since then, a number of circuit level features have been demonstrated for RFETs, which provide an added benefit over their CMOS counterparts: dynamic reconfiguration [60,61], intrinsic XOR [23] and wired-AND capabilities [15], control of threshold voltage [16], and suppression of parasitic charge sharing effects in dynamic logic gates [62,63]. Pioneering studies have proven, that this higher expressive capability of RFETs yields an added benefit on the circuit level, rather than the device level itself. In the predictive PDK by Gore et al. [64] 41% of area savings over the 10 nm FinFET process have been determined for a 1-bit full adder design, despite the larger individual transistor size. Similarly, Raitza et al. [65] have shown a 25% gain in critical path delay of a 16-bit conditional carry adder by reducing the number of stages and making efficient use of reconfiguration. Simultaneously with the increased amount of developments at the circuit level, the developments on the single device started to diversify in terms of material and transport physics. 2D layered systems, like graphene [13], black phosphorous [14], and transition-metal dichalcogenides, e.g. WSe_2 [12] or $MoTe_2$ [39,40] have been put into the focus in the last years. Small scale circuit demonstrators on these base materials have already catched up to the ones shown in silicon technology [66]. Also note, that they still follow the same technological principles as we have outlined earlier in Section 3, albeit the differences in their choosen channel material.

4.3. Towards electronic design automation for RFET circuits

An efficient circuit design based on RFETs requires the development of accurate models and the overall support of the electronic design automation. Efficient compact models have to be developed reflecting the physics of the device [64,67–70], which is distinctively different than that of classical MOSFETs, for example regarding the behavior of their parasitic capacitances [71]. Standard cell libraries have to be derived giving credit to the higher expressive capability of the RFET technology [72–75]. An early-level circuit analysis is extremely important to understand the efficacy of a particular emerging technology. This analysis usually requires a Verilog-A model of the technology which encapsulates the transistor's current and voltage properties. For reconfigurable nanotechnologies, various works such as [76,64,4] have been proposed which offer transistor-level models to carry out analysis for simple circuits. These models directly use laboratory level simulations and are helpful in understanding transistor's behavior at circuit levels. Fig. 4.

On the other hand, electronic design automation comprises primarily of two main stages – *Logic Synthesis* and *Physical Synthesis*. Fig. 5 shows the complete EDA flow and various approaches made in recent years to enable automated circuit design using RFETs. At the logic synthesis level, it has been shown that self-dual logic gates based on RFETs are a better choice for standard cells as they are more efficiently implemented with reconfigurable technology [77]. The same is true for the technology mapping stage [78], as well as physical synthesis flows. New data structures are needed to yield the full potential of these features [79,80]. In particular, logic synthesis exploiting self-duality during logic optimization leads to better area results for RFETs-based circuits [81].

However, in order to carry out a benchmark level analysis, technology-specific files in terms of.lef and.lib are required to enable top-down EDA flow. This is required to enable a standard-cell based ASIC flow for any emerging technology. One of the earliest works to enable a complete physical synthesis flow for emerging reconfigurable nanotechnologies was [74]. The authors used a 22 nm silicon nanowire-based model to characterize common logic gates such as AND, OR, MUX,

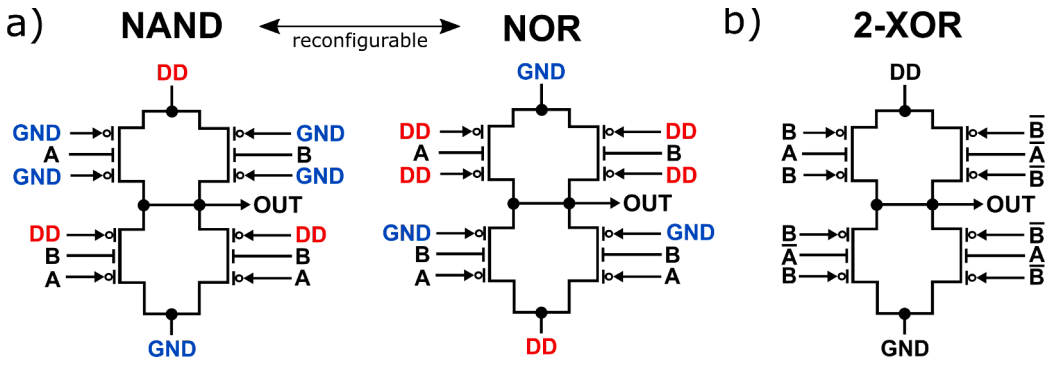

Fig. 4. Comparison of explizit and implizit reconigurability on the logic gate level on the example of (a) a reconfigurable NAND/NOR gate and (b) an compact functional-enhanced XOR gate.

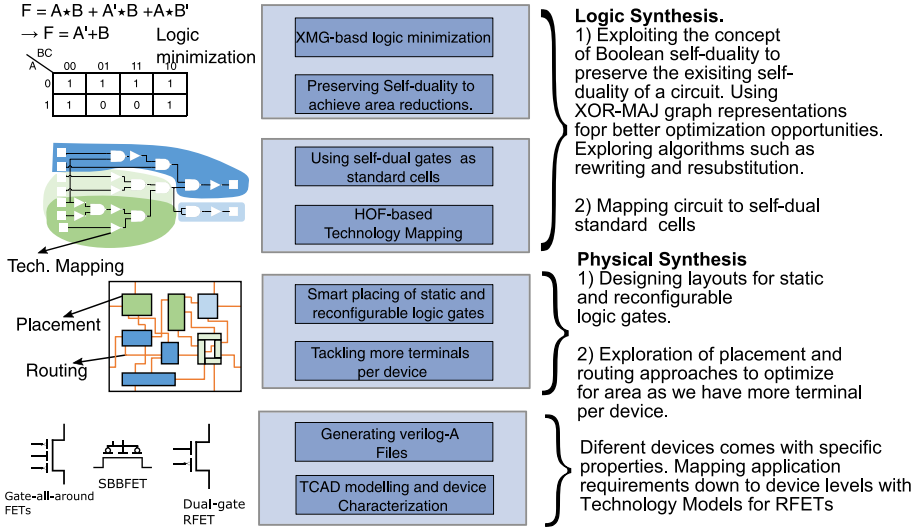

Fig. 5. Capable EDA flows are imperative for the overall development of RFET technology. This requires exploring techniques and approaches that can exploit their unique properties. We list down recent proposed approaches developed specifically for RFETs.

XOR, MIN etc. which can be used as standard cells in a typical EDA flow. Similarly, the authors in [72,73,82,83] proposed standard cell synthesis flow for other parallel RFET technologies.

5. Value-added features

Orthogonally to the shift of focus towards the circuit level, another trend is also rising over the last years: That is the combination of polarity-control with additional features, further enhancing the versatility of the RFET devices. The most discussed approach is a combination of the polarity control feature with a non-volatile storage option [84]. This trend comes quite naturally, as such a function is highly desired for enabling to permanently program the circuit's functionality, store weights in neuromorphic circuit applications, or for flexible computing-in-memory designs. Besides reconfigurability multi-valued logic (MVL) operations [85] are considered as another option to increase the system functionality, by replacing the conventional binary systems with operation schemes having higher radices or bases. One option to realize MVL are negative differential resistance (NDR) regions in the device characteristics. Recently, a realization of these NRD regions has been demonstrated in Al-Ge-Al nano-channels, showcasing a combination with the polarity-control feature of RFETs. These features will further enrich the possibilities of circuit designers employing RFETs and well be discussed in greater detail hereafter.

5.1. Non-volatile RFET concepts

The RFET concept was originally introduced to reversibly adjust the polarity of transistors at run-time. The polarity control is usually achieved by application of an additional static voltage which has to be constantly applied to maintain the function. Following the terms of the eponymous publication by Heinzig et al. [4], this voltage is often called program voltage, which selects the carrier-type (either electrons or holes) to be passing through the Schottky barrier. However, such operation is per definition volatile as the information is lost when the voltage is no longer applied. Thus, the term polarity gate yields a more precise description. Embedding a non-volatile option to these RFETs is an interesting concept as it would not only eliminate the requirement of the program voltage to be applied permanently but would also bring additional advantages in terms of multivalent memory operation or close proximity between logic and memory enabling new computing paradigms. The most used way to integrate such functionality is the addition of memory conserving layers in the gate stack of field-effect transistors. The most attractive candidates for such a storage element are charge-trapping [86] or ferroelectric [87] materials.

Several demonstrations of non-volatile RFETs have been reported in literature. First devices were realized by using charge trapping layers and silicon channels. In the first work by Schwalke et al., the buried oxide of a typical SOI sample was used as a charge trapping layer by applying high voltages to the global backgate [88]. Such operation is not suitable to individually address single devices while programming or

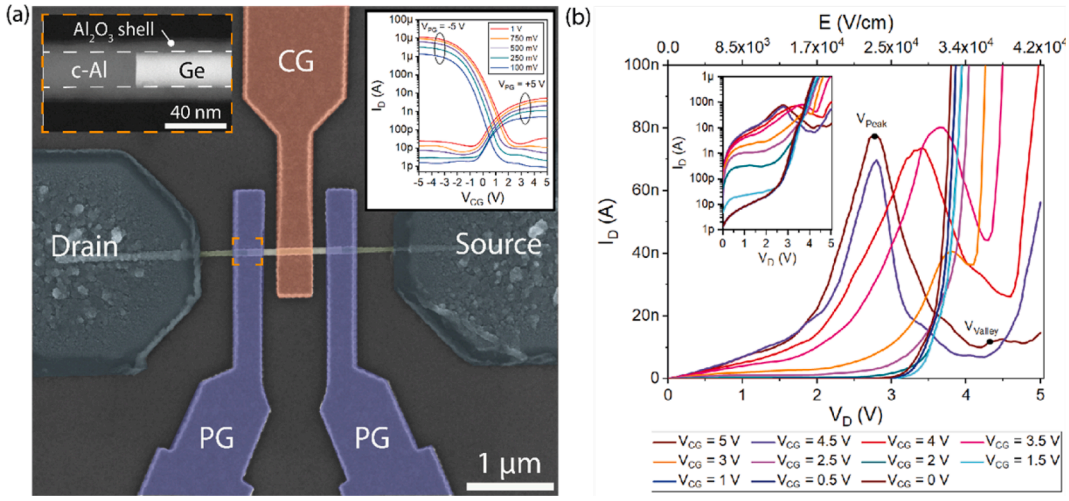

Fig. 6. (a) Colored SEM image of an Al-Ge-Al heterostructure embedded in a three-gate FET architecture enabling RFET operation and tunable NDR functionality. The left inset shows a high-resolution TEM image showing the entire Al-Ge interface of the NW heterostructure, where the Ge region is oriented in the [110] zone axis. The right inset shows the subthreshold transfer characteristic for different bias voltages between VD = 100 mV and 1 V showing unipolar p- and n-type operation programmed by VPG. (b) I/V characteristic of a RFET device with LGe = 1180 nm for VPG = 5 V and VCG voltages between 0 V and 5 V showing the gate-tunability of NDR with increasing VCG. The inset is showing a semi-logarithmic representation of the data.

erasing other devices. The next work by Park et al. used a programmable bottom-gate array and an oxide/nitride/oxide (ONO) stack for introducing nonvolatility [33]. This concept offers plenty of operation modes but requires complicated processing and the use of poly-Si channels. In 2017, the first demonstration of individually addressable non-volatile RFETs was published. In the work by Park et al., a bottom-up grown Si nanowire was used together with an MNO (metal nitride oxide) gate stack [86]. Successful programming and erasing for both n- and p-type modes enabled 4 distinct operation states for one single device. However, charge trapping requires high switching voltages and until now resulted in small memory windows. In order to improve these features, electrostatic doping by a ferroelectric polarization is frequently discussed [87,84,89]. As a first step towards this, it was shown by Sessi et al. that its possible to introduce non-volatility to a silicon nanowire SB-FET by integrating a thin doped ferroelectric HfO_2 film into the omega-shaped gate stack [90]. In this work, it was proven for the first time that it is possible to tune junction transmissibility by the programmed state. Due to the employed PtSi contacts hole conduction was more prominent and no typical RFET behaviour could be shown. A major drawback are the bottom-up grown silicon nanowires limiting reproducibility and scalability of the devices. The process was later adapted to a top-down silicon nanowires and successfully integrated ferroelectric hafnium-zirconium-oxide (HZO) into the gate stack of a single nanowire Schottky barrier transistor [91]. Tuning the on-currents by the ferroelectric polarization, this enabled an improved memory window of 1.5 V for hole conductance. A first successful demonstration of a ferroelectric RFET has been shown on 2-dimensional $MoTe_2$ channels, placing Copper-Indium-Thiophosphate (CIPS) at the polarity-gates only [92]. This material has however, only limited compability with standard-CMOS processes. Also, a fully functional device demonstrator exhibiting 4 distinctive operation states with ferroelectric programming still remains to be shown.

5.2. Ge based RFETs delivering negative differential resistance

Negative Differential Resistance is a property of some electrical devices in which an increase in voltage across the device's terminals results in a decrease in output current. Monolithic Al-Ge-Al channels [93–95] enable such a voltage controlled NDR transport [35] by the scattering of electrons from the energetically favorable low effective mass conduction band valley to a heavy mass valley nearby [96,97]. Although the L- and Γ-minima are energetically close in energy (0.66 eV vs. 0.8 eV), it was shown that the transferred electron effect more likely applies between the L- and X-minima rather than the L- and Γ-minima, with respective effective masses of $m_L^* = 0.082 * m_0$ and $m_X^* = 0.288 * m_0$ [98]. Interestingly, this tunneling process has not yet been observed in Ge hetero-structures with channel lengths below 100 nm, which is arguably due to the quasi-ballistic nature of transport in these elements [99]. However, RFETs' inherently longer gate length, due to the necessity of placing multiple gate terminals onto a single channel, make them the perfect platform for a combination with NDR effects [100]. In this work it has been shown that Al-Ge-Al-based devices can deliver a strong and reproducible NDR effect at room temperature as exemplified by the three-gated device shown in Fig. 6. As a result of this tunneling process, the output characteristics can be split into three regions: first the current increases (positive resistance) until it reaches a maximum at V_{peak}, then decreases in the region of negative resistance to a minimum V_{valley}, and finally increases again. For Al-Ge-Al heterostructure room temperature peak-to-valley ratios have been demonstrated which are about a factor of 20 times larger than that of existing Ge- or Si-based Esaki-diodes [101,102]. It was shown that both peak and valley voltages are independent of the investigated Ge nanowire diameter, but exhibit a linear-increase with the channel length. The reason for this trend is that with an increasing length, the series resistance of the device increases as well, and therefore shifts the whole NDR characteristic to higher voltages.

The voltage in the NDR region is a multi-valued function of the current making the NDR-mode highly desired for MVL gates, which target to replace conventional binary systems with operation schemes with higher radices [103]. Hence, implementing an operation scheme with higher performance using fewer devices and interconnects compared to standard CMOS circuits, owing to higher functionality of MVL circuits can be envisaged [104]. Recently, a new MVL concept based on exploiting the monostable-to-multistable [46] nature of serially connected NDR devices was demonstrated, creating a staircase of holding states [85]. An example for a simple yet innovative logic element taking advantage of the NDR characteristic is the monostable-bistable transition logic element (MOBILE) concept, employing two NDR devices connected in series capable to perform both NAND and NOR operations [94]. Furthermore, stacking more than two NDR devices, an efficient, and compact signed-digit NDR-based MVL adder combining a more than fivefold improvement in circuit propagation delay and a 15 times smaller area compared to common CMOS based

circuits has been proposed [105].

6. Future application potential

The versatility and flexibility provided by Reconfigurable Transistors poses them as powerful candidates for a number of applications. However, while some benefits or RFETs have been discussed for general computing, such as lowering area and activity of adder systems [65,64], or the elimination of the charge sharing effect in dynamic logic [62,63], they might not be powerful enough to replace CMOS as a whole. Thus, especially the co-integration of RFETs with classical MOSFETs stands out from an application point of view in the near future. In this way, RFETs can be applied as add-on functionality, where their special properties are beneficial, while the basic CMOS platform can be used to ensure system level performance. For this purpose it is convenient that RFETs can be built on nanoscale CMOS platforms without any changes required regarding the material or processes used [30]. The two most outstanding target applications for such a setup are hardware security and neuromorphic computing, which will be discussed in detail here after. Beyond that, the reconfigurable nature holds a lot of promises also for analog and mixed-signal designs [106,107,30], cryo-CMOS [108] as well as new operation schemes, such as asynchronous computing [77]. The combination of RFETs with NDR provides a prototyping platform for further potential applications such as fast switching Multi-Valued-Logic [104], bias-switchable positive/negative photodetectors with efficient dark-current suppression [37], or high-frequency oscillators [46].

6.1. Hardware security

Presently, a countless number of fabless-semiconductor companies are outsourcing their designs to offshore foundries. In this trend of globalization of integrated circuit design, there is a growing need to protect the designs from unauthorized access or untrusted users. During the production of an IC, from concept to fabrication, the process goes through a wide range of trusted and untrusted regimes [109]. As can be seen in Fig. 7, there can be multiple untrusted points in this global IC supply chain where adversarial attempts can be made to disrupt the design or make counterfeit copies. In any of the untrusted regimes, an attacker can gain access to the original netlist. Threats from the attacker can be categorised as: Hardware Trojans, IC piracy and over-production, unauthorised access to data, reverse engineering and counterfeiting [110].

Due to the increasing risk of hardware security breaches [111], there exists a growing need to strengthen hardware-level security to thwart such instances which could compromise the integrity of the ICs or even the original company's public image as well. Traditionally, various techniques of protecting the IP can be categorized in the avenues of watermarking, split manufacturing, camouflaging, logic locking schemes [109].

Logic locking schemes enhance hardware security across most of the avenues of an IC-supply chain. However, it is a trade-off between higher security vs. area and cost-overhead [112]. While there is an immense focus on developing newer algorithms for logic locking as well as all the other security measures, emerging devices are also being considered as potential candidates for replacing the CMOS-equivalent logic gates [113]. Among these emerging devices, RFETs show prominence to complement the CMOS gates, predominantly due to two features: functionality polymorphism and structural polymorphism [14]. This polymorphic nature enables new approaches on hardware security solutions, such as logic locking, camouflaging, physically unclonable functions (PUFs), or chip authentication [14,–116,77,117,118]. Also RFET-based logic cells and flip-flops are less prone to delay side-channel attacks (SCAs) than their CMOS counterpart [118,119], showcasing the potential for system hardening against outside attacks.

RFETs offer run-time reconfiguration which enables building polymorphic logic gates that, contrary to CMOS equivalent logic gates, can perform more than one function[25]. Logic locking with RFETs has been discussed in [120,112,114,121,14,117] which illustrates various polymorphic gates whose functionality can be reconfigured based upon the applied key values. Thereby, contrary to CMOS-based logic locking as presented in [122,123], RFET-based polymorphic gates can replace the logic gates of the original netlist, while satisfying the Boolean function as well as having a locking key to enable/re-configure the functionality of the entire circuit. Such functional-locking has additional advantages as compared to traditional CMOS-based logic locking. Due to the post-fabrication reconfigurability, reverse engineering the layout to obtain the original netlist becomes difficult for the attacker i.e. the uniform, planar layout of the fabricated design remains camouflaged [120]. RFET-based polymorphic locking gates, when placed in the original circuit design, reduce the area overheads and power-delay product significantly as compared to the CMOS-based locking algorithms [112,113].

Another interesting development came from the design of polymorphic logic gates with TIG-RFETs [23,124]. The authors in [125] showed the potential of using a TIG-RFET based multiplexer for a logic locking. It also describes the possibility to increase the key length per logic locking gate by using such multi-gated transistor architectures.

Besides logic locking, RFETs also show potential in other hardware security measures. In [120], the authors discuss the possibility of split manufacturing of the RFET-based logic gates, similar to the fabrication of CMOS equivalent gates. Thereafter, the correct functionality of the polymorphic gates built with RFETs can be selected in post-fabrication. In [118], the potential of RFETs to mitigate attackers from reverse-engineering the original netlist through side-channel attacks is illustrated. The authors propose XOR/XNOR logic functions with TIG-RFETs that show a reduction of power trace variations by 57%, the area overhead by 2 × , the switching power by 26% and the leakage by 8% when compared to CMOS equivalent logic gates. The prospective of

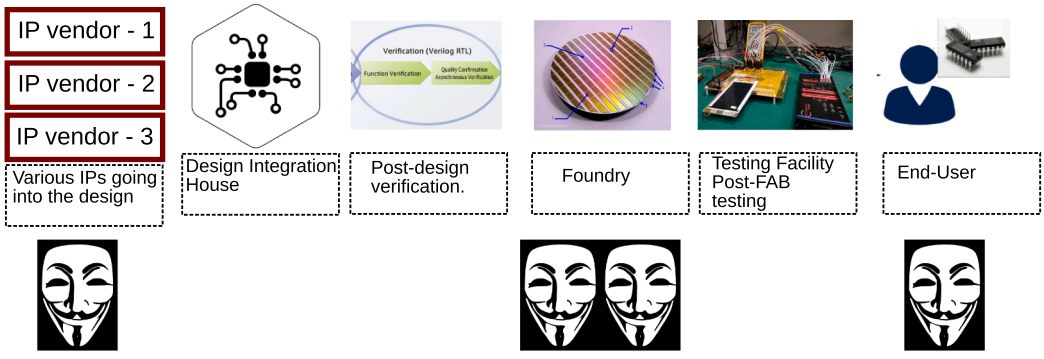

Fig. 7. Security from the perspective of global IC supply chain. Most vulnerable points are IP-vendors, foundry and the end-users. Of these, foundry is the most vulnerable point as various attack measures such as counterfeiting, over-production, insertion of hardware Trojans etc. can be realized.

reduction of power SCA with such reconfigurable logic gates arise from the symmetry between the output trace of different logic functions. On a similar basis specific design solutions have been proposed in [119] to equalize the propagation delay of both the operational modes of a NAND/NOR reconfigurable logic gates, leading to near delay-invariant designs. The remaining differences in the delay traces is hidden by the influence of process fluctuations [126], suggesting a high application potential in the field of securing circuits against timing SCAs.

Another interesting hardware security measure of watermarking was demonstrated in [61]. Here, the authors employed an approach where RFETs-based inverters are used for embedding watermarking scheme within a circuit. Due to the dynamic reconfigurability, the RFETs-based inverter demonstrates invariable logic as the inverter maintains its functionality for both values of program gate voltage (logic 1 and logic 0). This enables the hardware designer to use any kind of encoding scheme and embed it into the inverter logic to have a strong watermark. Further, owing to their dynamic reconfigurability, unlike CMOS, latches based on RFETs can deliver two metastable stages within a single clock cycle [127]. This allows generating random numbers at double the throughput as compared to an equivalent CMOS-based latch. All these concepts have to be further developed to be application relevant. Also a reliable process platform is needed prior to application. From the works listed above, one can already deduct that RFETs open a wide-range of new opportunities for hardware security due to being inherently secured against common attack-schemes.

6.2. Neuromorphic computing

The replication of information processing in neuronal biological systems is one of the main subjects of current research in electronics. The so called artificial neural networks (ANN) are superior to standard computing hardware in mimicking cognitive processes like pattern recognition, speech analysis, and system behavior prediction. In contrast to their biological counterpart, all state-of-the-art approaches are far less energy-efficient. The following properties of the biological system are radically different from standard electronics and contribute to the high efficiency of the brain's cognitive information processing: (1) It is massively parallel, three-dimensionally organised and very compact. (2) It combines storage and computation, (3) is fault-tolerant and robust and is (4) self-learning and adaptable to changing environments [128]. Standard nanoscaled devices in the commonly used von-Neumann architecture can mimic these characteristic only to some degree. A decisive property to standard electronics is the self-learning capability (4), also referred as adaptability or plasticity. Owing to the capability to change its function by an electrical stimulus, reconfigurable transistors inherent provide this ability to adapt their functionality. This enables the replication of the plasticity of biological neuronal units such as neurons and synapses already at device level. Also the generally lower on-currents of RFETs may pose a benefit instead of the drawback, when it comes to the aim of mitigating power consumption in highly parallel architectures. To this end, several reconfigurable device and circuit realizations have demonstrated, showing the ability for high-density synaptic operation. Typically, a combination of the polarity-control feature with an non-volatile storage option as discussed in Section 5.1 is required here. Further, the extended functionality given by certain gates can yield to more compact and efficient design. For example, the XNOR operation, which can be implemented very efficiently in RFET technology, represents the matrix–vector multiplication of binary neural networks (BNN) capable of simplifying computation and network complexity [129]. Bae et al. demonstrated that simple binary neural networks can be replicated using an area of only 8F2/synapse employing a 3-gate RFET (TIGFET) with Si_3N_4 charge storage layer as basic element [130]. Another simulation study by the same group also demonstrated 2-gate RFETs with Si_3N_4 charge storage layer as spiking neural network devices. In this way, an exponential relationship of the absolute drain current to the charges stored in the layer was demonstrated, leading to a near-linear relationship to the number of activation pulses. The short-term synaptic plasticity shows an energy consumption of 2fJ/spike, demonstrating high energy efficiency for an artificial synaptic device [131]. Reconfigurable threshold logic based on a single gate device with a floating body has been fabricated, providing linear and non-linear (XOR) Boolean functions on a 6F2 footprint exhibiting image recognition and edge detection capability [132]. A two-gated RFET circuit with synaptic spike time-dependent plasticity (STDP) and pulse-tuned synaptic potentiation or inhibition was demonstrated by Pan et al. based on the 2D semiconductor WSe_2 [133]. By tuning the potentials of the gates of the 2-gate RFET structure, similar to the design of Fig. 2e), the circuits can perform Hebbian and anti-Hebbian learning rules. The 3T1C design is less complex than an equivalent MOS circuit that would require 10 transistors for equal function. Similar excitatory and inhibitory responses could be achieved by reconfiguring the charge carrier transport over 2D heterostructures for different material combinations [134]. Fig. 8.

In addition to reconfigurability and charge storage, additional device properties are necessary to increase the performance and the energy efficiency of neuromorphic electronics. Such are an easy read and write accessibility in large networks, signal amplification, large fan-in and fan-out, interconnectivity, self-assembling ability, and easy to manufacture in large quantities at low cost [135]. As stated in Section 3, the device reconfigurability is not limited to a particular material, design, or manufacturing process. Therefore various technologies can be explored to combine these requirements with a reconfigurable device to get closer to the efficiency of the biological equivalent.

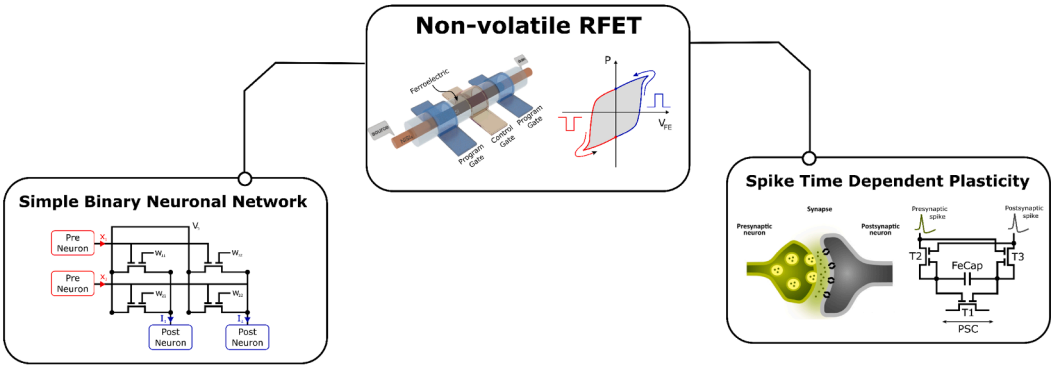

Fig. 8. Neuromorphic Computing with RFETs. (a) Schematic of a three-gated RFET with added non-volatile storage option by placing a ferroelectric material within the gate dielectric as enabler for neuromorphic circuit designs. (b) circuit diagram of a simple Binary Neuronal Network realized by RFETs (c) circuit diagram of a synapse able to realized spike-time-dependent-plasticity. (d) Generic representation of a biological synapse.

7. Conclusion

The basic concepts that have lead to the development of RFET devices have been introduced more then 20 years ago. Meanwhile, the field has continuously developed. While device demonstrations were in the focus for the first years, the research activities have extended towards device optimisation and circuit applications. Here, a solid understanding on how to construct optimized devices and how to implement circuits that can bring a significant advantage over conventional solutions is available. However, even if significant steps have been taken, it will be a long journey to introduce full reconfigurable circuits based on such devices into industry as it will require significant changes in the design methodology and the design flow. Therefore, applications that can enrich integrated circuits by adding RFETs to the standard CMOS process are of huge interest in order to create a first step for the industrial application of this novel type of devices. Recently, it has been demonstrated that such devices can be integrated with very low process overhead into advanced CMOS processes. This is a prerequisite to have RFETs as an add-on device rather than substituting classical devices. For such an approach, hardware security and neuromorphic applications can be attractive entry points. From there on, the application of RFETs devices could then extend in two dimensions namely adding new device functionalities like non-volatility and extending the circuit applications towards run-time reconfigurable circuits. In summary, RFET devices have moved from the basic concept to a well understood add-on device in the last 20 years. They offer a large number of options for further complexity increase of integrated circuits that is continuously extended by novel research approaches and needs to be funneled into real world applications in the upcoming years.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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