CVD-GFETs with Record-small Hysteresis Owing to 2nm Epitaxial CaF$_2$ Insulators

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Introduction: Graphene is a promising material with numerous properties [1] which can be exploited in optoelectronics [2] and sensors [3]. Many of these devices require high-quality insulators to either form graphene FETs (GFETs) [2, 3] or otherwise protect graphene. Previously used amorphous oxides contain numerous border traps [4] which cause severe hysteresis and long-term drifts of the gate transfer characteristics [5]. As a promising alternative, here we demonstrate GFETs with 2nm thick CaF$_2$ insulators previously used in the most stable MoS$_2$ FETs reported so far [6]. CaF$_2$ is an ionic crystal insulator with good dielectric properties ($\varepsilon = 8.43$, $E_g = 12.1$eV) which forms quasi van der Waals interfaces with 2D materials [7]. We examine >100 GFETs with different sizes and perform a detailed study of the hysteresis dynamics which is used as the key figure of merit to benchmark the device stability. After minimizing the impact of non-insulator defects by annealing at 175°C, we demonstrate that the stable clockwise hysteresis in our GFETs with CaF$_2$ is orders of magnitude smaller than in GFETs and MoS$_2$ FETs with SiO$_2$ and Al$_2$O$_3$.

Devices: Our devices are single-layer GFETs fabricated by conventional photolithography on Si/CaF$_2$ substrates (Fig.1a) prepared by our established molecular beam epitaxy method at 250°C [8]. To avoid leakage currents from large contact pads, they have been isolated with 10nm Al$_2$O$_3$ grown by plasma assisted atomic layer deposition just before sputtering of the 25nm Pd electrodes. Next, a commercial CVD-graphene was transferred onto the substrate by a PMMA assisted method and patterned by oxygen plasma. The obtained arrays contain hundreds of GFETs with channel dimensions ($L \times W$) from 160 $\mu$m $\times$ 100 $\mu$m down to 9 $\mu$m $\times$ 3 $\mu$m. Typical $I_{D,0}$-$V_{G}$ characteristics (Fig.1b) exhibit relatively high currents up to 32 $\mu$A/µm within few Volts operation range due to the highly downscaled thickness of the gate insulator at only 2nm. The $I_{D,0}$-$V_{G}$ characteristics (Fig.1c) show good current control with some kinks typical for ambipolar GFETs. We have also fabricated similar back-gated GFETs on Si substrates with 90nm SiO$_2$ and 36nm Al$_2$O$_3$ to serve as a reference for comparison of the hysteresis.

Results and Discussions: In Fig.2a we show that already at this early stage of research many GFETs with very similar $I_{D,0}$-$V_{G}$ characteristics can be obtained. The analysis of $I_{D,0,ac}$ vs. $V_{D,0,ac}$ distributions for 116 studied devices (Fig.2b) shows that the variability is stronger for smaller channels which are likely more affected by grain boundaries in CVD-graphene. In Fig.3 we analyze the hysteresis dynamics in GFETs with 80 $\mu$m $\times$ 50 $\mu$m channels. Among five selected devices, there is one “Golden” which exhibits considerably higher $I_{D,0}$ (Fig.3a), likely because of fewer grain boundaries within the channel. The hysteresis width ($\Delta V_{H}$) vs. reciprocal sweep time ($1/v_{sweep}$) dependences [9] measured for these GFETs are shown in Fig.3b. All devices exhibit switching of the hysteresis from counterclockwise at faster sweeps to clockwise at slower sweeps. Remarkably, the hysteresis is much less pronounced for the “Golden” GFET which may thus serve as a benchmark for further technology improvement. To understand the origin of the observed hysteresis dynamics, we perform a similar analysis on smaller devices. The results shown in Fig.4 suggest that despite the overall variability in $\Delta V_{H}(1/v_{sweep})$ curves, some devices with different sizes may have nearly identical hysteresis dynamics. Thus, this variability is not directly related to the channel dimensions but rather to the local quality of the channel. At the same time, it is remarkable that some of these smaller GFETs exhibit a counterclockwise hysteresis even at slow sweeps, while the others have purely clockwise hysteresis which increases for slow sweeps.

In Fig.5 we analyze the observed difference in hysteresis dynamics by examining GFETs with counterclockwise (Device 1) and clockwise (Device 2) hysteresis at different T up to 175°C and back at 25°C after few days of annealing at 175°C. Indeed, the counterclockwise hysteresis can be considerably suppressed, which makes the initially different $\Delta V_{H}(1/v_{sweep})$ traces of two GFETs nearly identical after annealing. This suggests that the counterclockwise hysteresis is likely due to some adsorbates trapped at the grain boundaries, thus being less pronounced for GFETs with more homogeneous channels which explains the initial variability. Thus, the true hysteresis coming from charge trapping by border defects in CaF$_2$ is the clockwise one which we observe after annealing. In Fig.6 we benchmark these $\Delta V_{H}(1/v_{sweep})$ traces normalized by the insulator field factor against the results measured for MoS$_2$ FETs with SiO$_2$ [10] and CaF$_2$ [6], and also our reference GFETs with SiO$_2$ and Al$_2$O$_3$. Indeed, owing to the low defect density in crystalline CaF$_2$, the hysteresis in our GFETs is orders of magnitude smaller than in devices with oxides, just like in MoS$_2$/CaF$_2$ FETs [6].

Conclusions: We fabricated hundreds of CVD-GFETs with 2nm epitaxial CaF$_2$ insulators and performed an in depth study of the hysteresis. Our results show that while the grainy structure of the channel may introduce variability in device performance and hysteresis dynamics, a vacuum anneal at 175°C results in record-small hysteresis. This confirms that the use of thin crystalline CaF$_2$ is a promising way to enable stable GFETs for sensors and optoelectronics.

Fig. 1: (a) Schematic structure of our back-gated GFETs with 2nm CaF₂ insulators. (b) Typical \(I_D-V_G\) characteristics of these devices. The inset shows that the gate leakage current through our thin CaF₂ layers is small compared to the drain current. (c) The \(I_D-V_G\) characteristics measured for the same GFET exhibit some ambipolar kinks.

Fig. 2: (a) \(I_D-V_G\) characteristics of 11 similar GFETs with 50μm x 50μm channels selected from our total statistics of 116 devices with different channel dimensions. (b) The distribution of \(I_{Drac}\) vs. \(V_{Drac}\) for all 116 devices; the number of devices with the corresponding channel dimension is marked in brackets in the legend. The measurements have been done before any annealing step, and some smaller devices have a more positive \(V_{Drac}\) (for those GFETs we used \(V_G\) sweep range from 0 to 4 V).

Fig. 3: (a) Double sweep \(I_D-V_G\) characteristics of 5 GFETs with 80μm x 50μm channels measured using ultra-slow sweeps with \(S = 0.002\) V/s. Among these devices, there is one “Golden” device with considerably larger current and near-zero \(V_{Drac}\). (b) The \(\Delta V_H\) vs. \(1/f_{sw}\) dependence for the same GFETs. Compared to typical devices, the “Golden” device has smaller clockwise hysteresis at slow sweeps and almost no counterclockwise hysteresis at fast sweeps.

Fig. 4: (a) Double sweep \(I_D-V_G\) characteristics of GFETs with 40μm x 20μm (top) and 9μm x 3μm (bottom) channels measured with different sweep rates. The hysteresis dynamics observed for these two devices are very similar. (b) The \(\Delta V_H\) vs. \(1/f_{sw}\) dependence for 7 GFETs with different channel dimensions. While there is some variability in the hysteresis dynamics, some devices with different sizes have identical hysteresis and thus this effect is independent of the channel dimensions.

Fig. 5: (a) Double sweep \(I_D-V_G\) characteristics measured at \(T = 25^\circ\)C, 175°C and 25°C after annealing using \(S = 0.002\) V/s. Initially Device 1 (top) exhibited counterclockwise and Device 2 (bottom) clockwise hysteresis. (b) At 100°C and then 175°C the counterclockwise hysteresis in Device 1 is strongly suppressed (left), and after annealing at 175°C both devices exhibit similar clockwise hysteresis (right).

Fig. 6: The normalized clockwise hysteresis in our GFETs with CaF₂ is orders of magnitude smaller than in all devices with oxides, being similar to previously studied MoS₂ FETs with 2nm CaF₂.