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About electron transport and spin control in semiconductor devices

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ABSTRACT

As the scaling of CMOS-based technology displays signs of an imminent saturation, employing the second intrinsic electron characteristics – the electron spin – is attractive to further boost the performance of integrated circuits and to introduce new computational paradigms. A single electron spin forms a qubit and is suitable for quantum applications. In digital applications, the spin promises to offer an additional functionality to charge-based CMOS circuitry. Recently, spin injection into a semiconductor and spin manipulation by the gate voltage were successfully demonstrated providing a vision that devices using spin in addition to charge may appear in significant numbers on the market in the non-distant future.

On the memory side, the nonvolatile CMOS-compatible spin-transfer torque (STT) and the spin–orbit torque (SOT) magnetoresistive random access memories (MRAMs) are already competing with flash memory and SRAM for embedded applications. A combination of nonvolatile elements with CMOS circuitry allows to shift the data processing into the nonvolatile segment, paving the way for a novel low power computational paradigm based on logic-in-memory and in-memory computing architectures.

To model MRAM, we innovatively extend the spin and charge transport equations to multi-layered structures consisting of normal and ferromagnetic metal layers separated by tunnel barriers. We validate our approach by modeling the magnetization dynamics in ultra-scaled MRAM cells.

1. Introduction

Continuous miniaturization of metal–oxidesemiconductor field effect transistors (MOSFETs) is one of the main drivers ensuring the impressive increase in speed, performance, density, and complexity of modern integrated circuits. Numerous outstanding technological challenges have been resolved on the exciting journey of continuous transistor downscaling. At all stages, accurate TCAD tools were paramount to predict the device functionalities, to optimize the parameters, and to obtain the best performance. To describe the electron transport, the drift–diffusion model enjoyed a remarkable success at earlier stages of MOSFETs modeling due to its relative simplicity, numerical robustness, and the ability to perform two- and three-dimensional simulations on large unstructured meshes [1].

Since the 90 nm technology node, strain as a MOSFET channel mobility booster was introduced [2]. This allowed improving the on-current while maintaining other characteristics including the off-current unchanged. To improve the on-current in *n*-silicon channels, tensile capping layers are used. In *p*-channels compressive capping layers are complemented by epitaxially re-grown SiGe source and drain enhancing strain [2]. The simulation tools incorporated corresponding strain-enhanced mobility models which were carefully tailored with the help of accurate band structure calculations of strained Si [3].

To proceed to the 45 nm CMOS technology node, the electrostatic channel control was improved by replacing the native SiO_2 gate oxide with a high permittivity HfO_2 dielectric and metal gates [4]. The use of HfO_2 allowed to maintain the physical gate oxide sufficiently thick to suppress parasitic tunneling leakage currents. However, to preserve a good electrostatic channel control at the 22 nm technology node, a new architecture of three-dimensional tri-gate transistors was required [4]. Importantly, the doping of three-dimensional fins became unnecessary as the electron confinement in the channel is geometrical and not due to depletion. This allowed to make the fins taller and thinner, which, in combination with strain and high-k dielectrics/metal gates, allowed to scale the technology down to 14 nm [5] and 10 nm [6]. By introducing pitch splitting, self-aligned patterning, and EUV lithography the transistor miniaturization was continued down to 7 nm feature size [7]. Using full-fledged EUV lithography and high mobility channel FinFETs,

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the 5 nm technology node provides ~ 1.8x improvement in logic density, 15 % speed gain, and 30 % power reduction compared to its previous generation [8]. For upcoming technology nodes, gate-all-around devices are optimal candidates. To sustain the high on-current through the transistor, the channel in such devices should contain several nanosheets surrounded by the gates [9].

To model such devices, quantum effects including a confinement must be included [10]. When modeling the transport in ultra-scaled fins with only a few subbands occupied, a full subband method [11] must be applied.

For sufficiently long transistor channels the carrier motion in transport direction can be treated semi-classically, and the use of transport models based on a set of coupled subband Boltzmann transport equations is sufficient [12]. In ultra-scaled MOSFETs, however, the transport becomes ballistic and is determined by several transversal propagating modes in the channel. The channel conductance ceases to depend on the channel length. The supply voltage does not decrease with the channel length [13]. This results in an approximately constant power dissipation of a single MOSFET. The generated heat per area increases rapidly with increasing transistor density, which puts a foreseeable limitation on scaling.

2. Electron spin as a computational degree

As the downscaling of charge-based CMOS devices is approaching its saturation, the electron spin attracts attention as a suitable candidate for complementing or even replacing the electron charge in future microelectronic devices [14–16]. The electron spin can point in any direction on a Bloch sphere. A single spin is suitable to build a qubit. Two or more qubits can be in an entangled state. This state cannot be represented as a direct product of independent qubit states. The entangled state cannot be described by classical mechanics. Therefore, using qubits for quantum information processing is a key for achieving a superiority of a quantum computer over a classical one for certain applications. Single-spin qubits in semiconductors are realized with impurities [17] or quantum dots [18]. The quantum dot technology was recently shown to have a potential towards utilization in a large-scale quantum computer. Three-dimensional silicon quantum chips were demonstrated, in which a precise interlayer alignment is achieved guaranteeing highly accurate manipulation and detection of the spin states [19]. A successful implementation of a quantum computer based on spins requires the capability of efficient spin initiation, coherent manipulation, and reliable read-out [20]. An unprecedented advantage in these fields has been demonstrated with the successful realization of a two-qubit quantum gate [21] and a quantum processor with a fidelity exceeding 99 % [22]. The pressing challenge now is to proceed to a larger computational network of qubits. Employing quantum dots is an attractive option due to their similarity to scaled transistors providing the perspective to integrate spin qubit devices on a 300 mm wafer [23].

Single-spin qubits diamond and SiC demonstrate a spin coherence time of several microseconds even at room temperature [24]. In addition, the electron spins can be coupled to nearby nuclear spins with a long coherence time. Recently, a three-qubit quantum processor [25] as well as a ten-qubit solid-state spin register with a long- time stable quantum memory up to one minute [26] were demonstrated. The technology, however, requires a controllable creation of defects with long-living spin states, which represents a significant challenge in modern semiconductor technology. A recent roadmap on quantum nanotechnologies including spin is available [27].

The stationary spin state is characterized by one of the two possible projections on a given axis defined by a magnetization direction. These two states can be used for digital data processing. The status of spin augmented electron switches as well as spin current enabled magnetoresistive random access memories (MRAM) complemented with our modeling approach is discussed next.

3. SpinFETs and SpinMOSFETs

A spin field-effect transistor (SpinFET) [28] employs the spin polarization to enrich the transistor performance. A SpinFET is composed of a semiconducting channel region sandwiched between ferromagnetic source and drain. The source contact injects spin-polarized electrons in the channel. The drain magnetization is used to detect the spin polarization of the electric current. If the magnetization of the drain is parallel to that of the source the spin-polarized electrons easily escape from the channel to the drain, and the current is large. If the source and drain magnetizations are anti-parallel, the current is small. SpinFET potentially opens a path to a reconfigurable logic [29], spin-based complementary logic devices [30], and muti-gate SpinFET logic [31] Experimentally, a large absolute (but not relative) difference between the two values of the on-currents for parallel and anti-parallel source-drain orientations was recently observed in a Si MOSFET at room temperature [32]. It proves that the spin relaxation in silicon at room temperature is sufficiently weak. It can be further suppressed by using stress [33], the technique applied to boost the carrier mobility in Si [2].

When the current flows a ferromagnetic metal, the supply of both spin-up and spin-down electrons in the semiconductor is overwhelmingly high. Both states with spin-up and spin-down are equally populated, and the current running through the semiconductor remains unpolarized. To overcome this spin conductivities mismatch [34], metal ferromagnetic source and drain were connected to silicon channel in [32] through tunnel contacts. The tunnel barrier reduces the electron flow to make the population of the spin-up/spin-down states proportional to the majority/minority electron density in the ferromagnet [35].

The demonstrated device [32] is not a real SpinFET proposed in [28] as the (back)gate only serves to turn the electric current on or off. The proposal [28] constitutes an all-electric, not magnetic way to manipulate spins by an effective gate voltage dependent spin–orbit field [36]. This spin–orbit field makes the injected spin polarization to rotate at a certain angle while the spins are propagating in the channel under the gate. As the spin–orbit field depends on the fate voltage, the angle can be controllably adjusted. In addition, The spin–orbit field depends on the electron momentum. It guarantees that all ballistically propagating spins acquire the same rotation angle [28] at the end of the channel.

To demonstrate a SpinFET one should have a semiconductor with a strong spin–orbit interaction. The spin–orbit interaction is several orders of magnitude larger in III-V semiconductors compared to the one in Si making them good candidates to build SpinFETs. However, a strong spin–orbit interaction also results in a strong spin relaxation. Therefore, a SpinFET made with III-V channels can only operate at low cryogenic temperatures. Additionally, for a successful demonstration of the gate-induced spin precession it is necessary to avoid ferromagnets in the device as they cause stray fields resulting in spurious current oscillations. An elegant solution to the problem of injecting spin-polarized electrons without using ferromagnetic contacts has recently been [37] proposed. The effective spin–orbit field [36] guarantees that the moving electrons become automatically spin-polarized. Injecting spins through a point contact biased with a normal electric field created by additional gates results in spin-polarized injection currents. Using this injection technique, the current modulation at cryogenic temperatures by means of the gate–voltage-dependent spin–orbit field was confirmed [37]. The first proof-of-concept demonstration of a SpinFET came 25 years after it was predicted [28].

Although fundamental problems and technological challenges to demonstrate the spin injection, spin propagation, spin manipulation, and spin detection in a semiconductor channel have been experimentally verified to demonstrate first prototypes of a SpinFET and a SpinMOSFET, their characteristics and modes of operations are not very impressive. In particular, the ratio of the current difference in parallel and anti-parallel configurations to the current in a Si SpinMOSFET is only about 10^{-5} [32]. To increase the ratio, both the spin injection efficiency by the source and the spin detection efficiency by the drain must

be increased, while the spin relaxation is suppressed. The injection and detection can be optimized by tuning the tunnel barrier's transparency and its spin filtering efficiency. However, even for optimal barriers on silicon the experimental efficiencies are about 15 % [38] resulting in a magnetocurrent ratio of 5 %.

The spin injection schemes still rely on the charge current. Therefore, both, the SpinFET and the SpinMOSFET, are prone to the same scaling limitations as CMOS FETs. New innovative solutions for purely electrical efficient spin injection and manipulation are urgently needed to help spin-based switches to reach maturity.

A promising avenue is to explore unique properties of novel two-dimensional materials. Recently, it has been shown that both the gate voltage and the in-plane electric field in a sheet of tungsten di-selenide bonded on a sheet of bilayer graphene are capable to change the polarization of the spin current up to room temperature [39]. An alternative path is to explore devices with already large magnetoresistance.

4. Emerging magnetoresistive memories

A magnetic tunnel junction (MTJ) is a sandwich made of two ferromagnetic contacts separated by a tunnel junction. The tunnel magnetoresistance ratio in MTJs can reach several hundred percent at room temperature [40]. Due to the large difference in the resistances of the parallel and anti-parallel MTJ configurations, MTJs are suitable for storing the binary data. The typical resistance of an MTJ is similar to that of a MOSFET. It makes MTJ-based magnetoresistive random access memory (MRAM) electrically compatible with CMOS circuitry without extra amplifiers to convert the spin (magnetization) degree into charge. The spin-transfer torque (STT) effect [41,42] has been shown to be perfectly suitable for the electrical data writing. Indeed, the magnetization of a free layer (FL) can be changed between the two orientations parallel and antiparallel to the magnetization of the fixed layer by passing an electric current through an MTJ.

STT-MRAM is considered as a perfect candidate for future universal memory. STT-MRAM is fast (10 ns), it possesses high endurance (10^{12}), and it has a simple structure. It is compatible with CMOS technology and can be straightforwardly embedded in circuits [43]. STT-MRAM solutions compatible with 22 nm FinFET [44] for last level caches and 16 nm FD SOI [45] embedded MRAM technologies are available. A recent annual report [46] implies that the particular company is developing a scaled MRAM option to replace SRAM memory. At the same time, embedded MRAM is also positioned as a replacement for configuration memory.

An MRAM cell consists of several layers, including CoFeB ferromagnetic reference and free layers separated by an MgO tunnel barrier. To increase the perpendicular magnetic anisotropy, the FL, typically composed of two CoFeB layers and a thin metal buffer, is interfaced with the second MgO layer [47]. Introducing more CoFeB/MgO interfaces [48] and elongating the FL allows to boost the perpendicular anisotropy even further, while reducing the FL diameter [49].

For an accurate design of ultra-scaled MRAM cells it is paramount to evaluate the magnetization dynamics in elongated ferromagnetic layers. To compute the torques acting on the magnetization, the nonequilibrium spin accumulation must be evaluated. For this purpose, the coupled system of the spin and charge transport equations must be solved. As charge and spin transport depend on the instantaneous magnetization configuration, the torques are evaluated by solving the coupled system of transport equations and magnetization dynamics.

The ferromagnetic layers in ultra-scaled MRAM cell pillars [49] are elongated along the easy magnetic axis and cannot be approximated by two-dimensional discs. Therefore, a modern TCAD tool for designing ultra-scaled MRAM cells must solve the key equations for magnetization dynamics in three dimensions.

The FL may consist of several elongated ferromagnetic pieces separated by MgO tunnel barriers and/or normal metal buffers. The FL is separated from the fixed magnetization layer and the cupping layer by MgO tunnel barriers. Therefore, the TCAD tool must properly evaluate the charge and spin transport through ferromagnetic layers separated by tunnel barriers and normal buffer layers to describe simultaneously the interface-like torques [41,42] and the bulk torques due to the magnetization gradients.

The magnetization dynamics in ferromagnetic layers separated by a metal layer is accurately described by the Landau-Lifshitz-Gilbert equation coupled to the charge and spin drift–diffusion transport model [50]. We have generalized the spin and charge drift–diffusion model to incorporate the tunnel barriers [51]. The method treats the interface-like torques [41,42] and the torques acting on the textured magnetization in elongated ultra-scaled FLs on equal footing. The spin and charge transport approach [51] coupled with heat flow [52] was applied [53] to double reference layer STT-MRAM [54]. The generalization allows to describe spin–orbit torques (SOT) [55] in SOT-MRAM, another highly promising emerging memory [56].

5. Conclusion

A successful adoption of the electron spin in microelectronics can potentially revolutionize data processing by, e.g., introducing spin-based qubits and the use of the electron spin in digital switches. Both fields are still in the fundamental research phase, just the emerging magnetoresistive memories already employ the spin currents for their operation. MRAM is fast nonvolatile, and CMOS-compatible. Developing logic-in-memory architectures suitable for in-memory processing will inevitably improve ultralow-power electronics, Big Data analysis, automotive electronics, and the Internet of Things. The electron spin can also be expected to have an enormous impact on neuromorphic computing and artificial intelligence of things.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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